Fully depleted CCD's Fabricated on High-Resistivity Silicon

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Fully-depleted CCD technology

Background

- Motivated by SuperNova Cosmology Group
- Spin off of high-energy-physics detector R&D
- Fabrication at LBNL Microsystems Laboratory

Summary of 2k x 2k Results

- Quantum efficiency > 80% at 950 nm
- Excellent charge transfer efficiency (> 0.999995)
- Point spread function Gaussian with σ ~ 10 µm at V_{sub} = 35V

Recent Results/In Progress

- Demonstration of ~ 2 e- rms noise at 8 µs sample time
- Demonstration at 800 x 1980 CCD at NOAO KPNO 4m RC spectrometer
- 200 µm thick CCD PSF measurements at Lick Hamilton Spectrograph
- Preliminary proton irradiation results
- First results at 150 mm wafer foundry (photodiodes)
- Submission of 150 mm wafer CCD layout including test CCD's for 10 MHz readout, 9 µm pixel CCD's, and 4 quadrant readout

LBNL MicroSystems Laboratory

- Conceived by the LBNL Physics Division to support the detector R&D effort for the Superconducting SuperCollider
- Class 10 clean room dedicated to high-purity silicon fabrication
- Includes full CCD fabrication capability except ion implantation (3 commercial vendors in the Bay Area)
- Equipment includes:
    - 1X lithography for large area CCD development (Intel donation)
    - Polysilicon and silicon nitride dry etching (partially funded by Keck Telescope Science Steering Committee)
    - Oxidation and annealing furnaces
    - Polysilicon, silicon nitride, and silicon dioxide thin film deposition furnaces
    - Aluminum, silicon dioxide and indium tin oxide deposition (sputtering)
- 100 mm wafer facility although some equipment can be upgraded to 150 mm
- Successful fabrication of 200 x 200, 2048 x 2048, and 2048 x 4096 $(15\mu m)^2$ CCD's

LBNL Microsystems Laboratory

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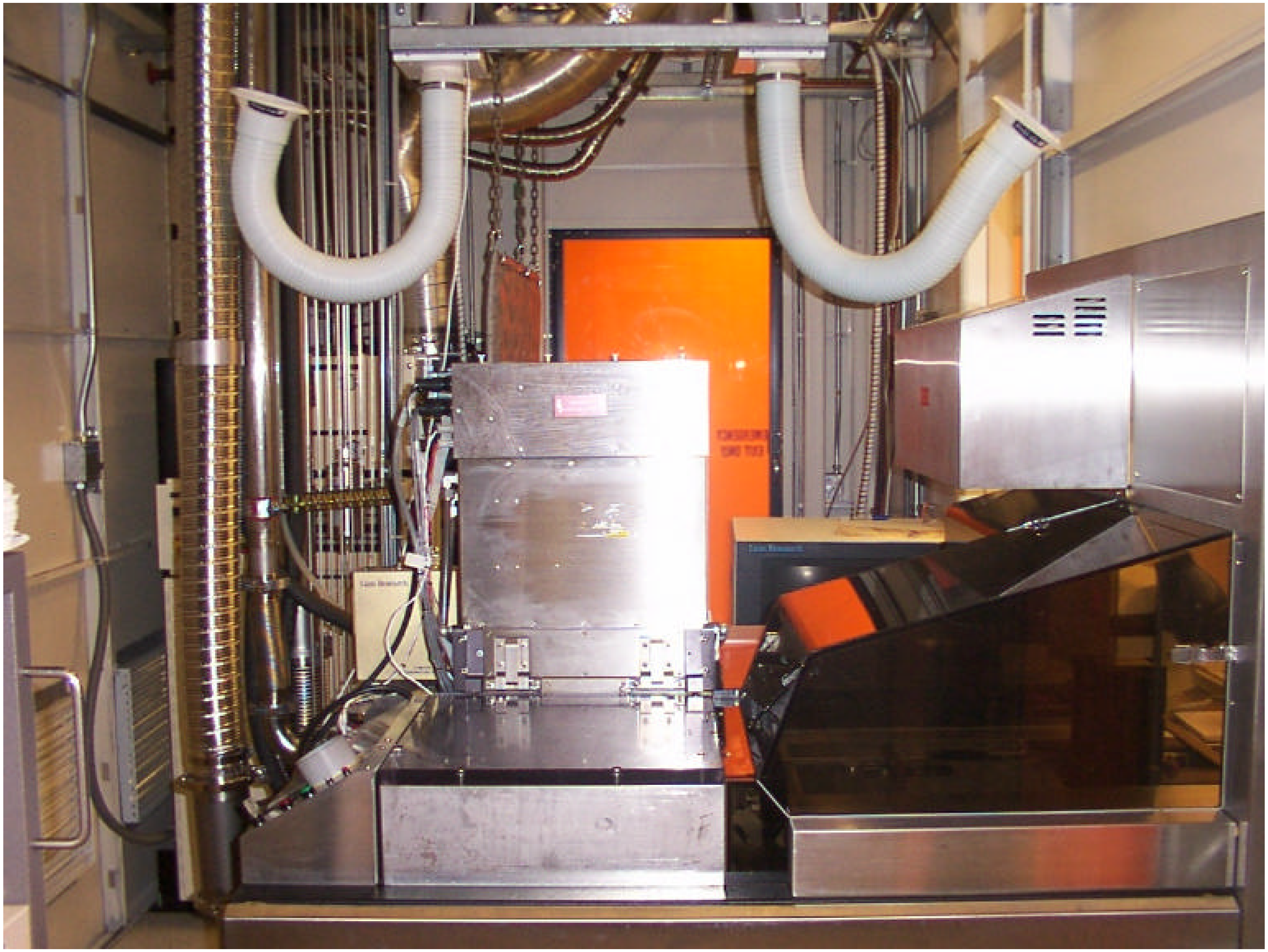
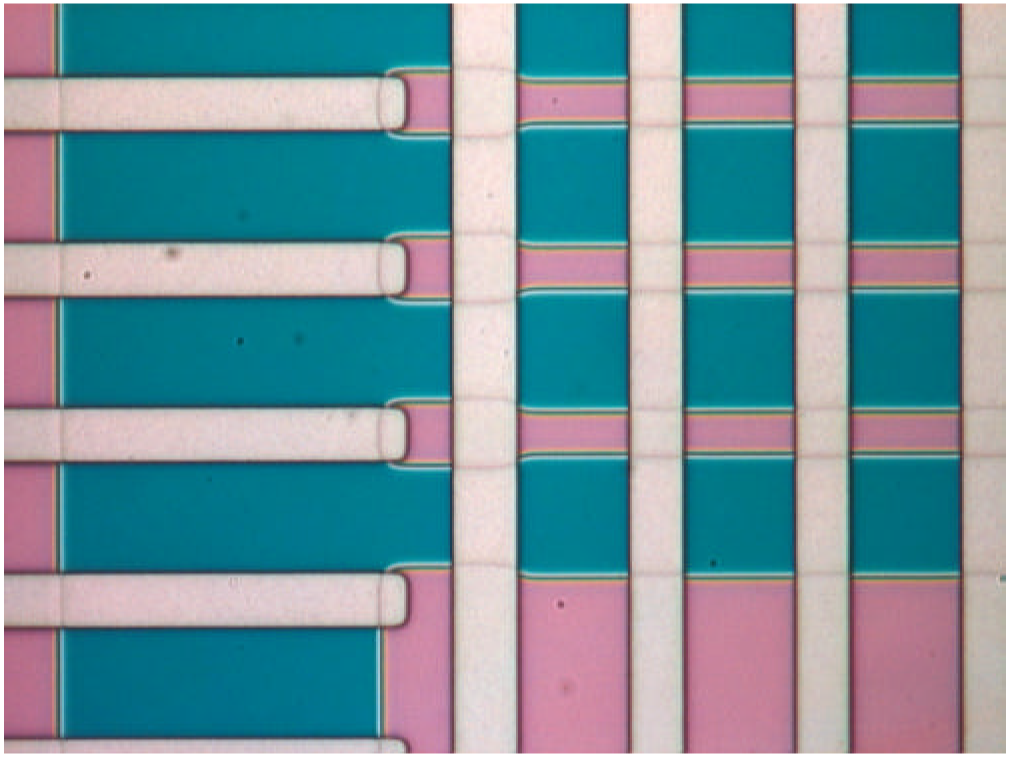
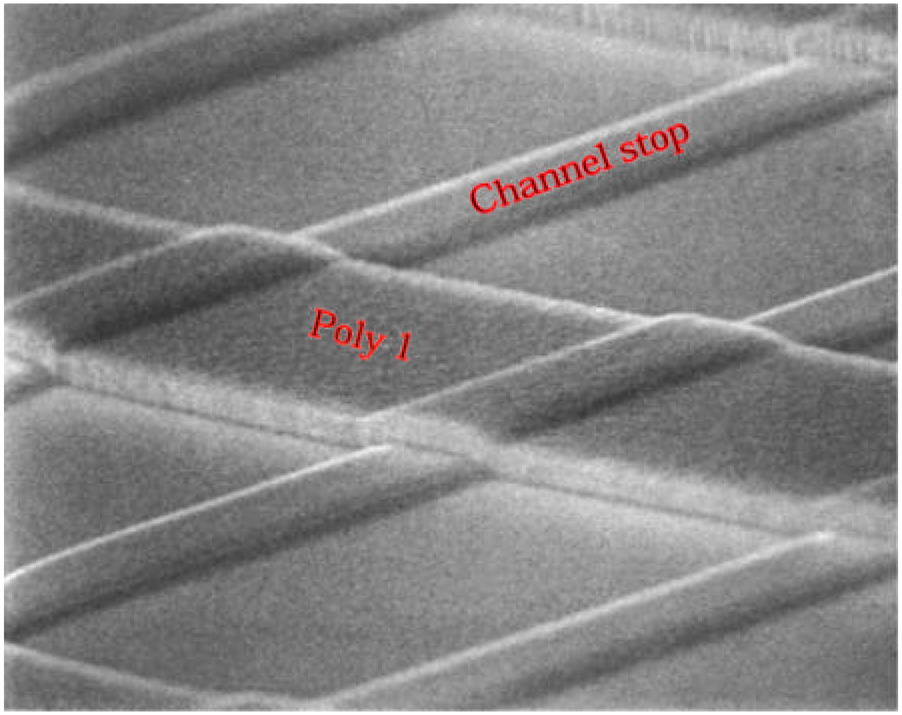


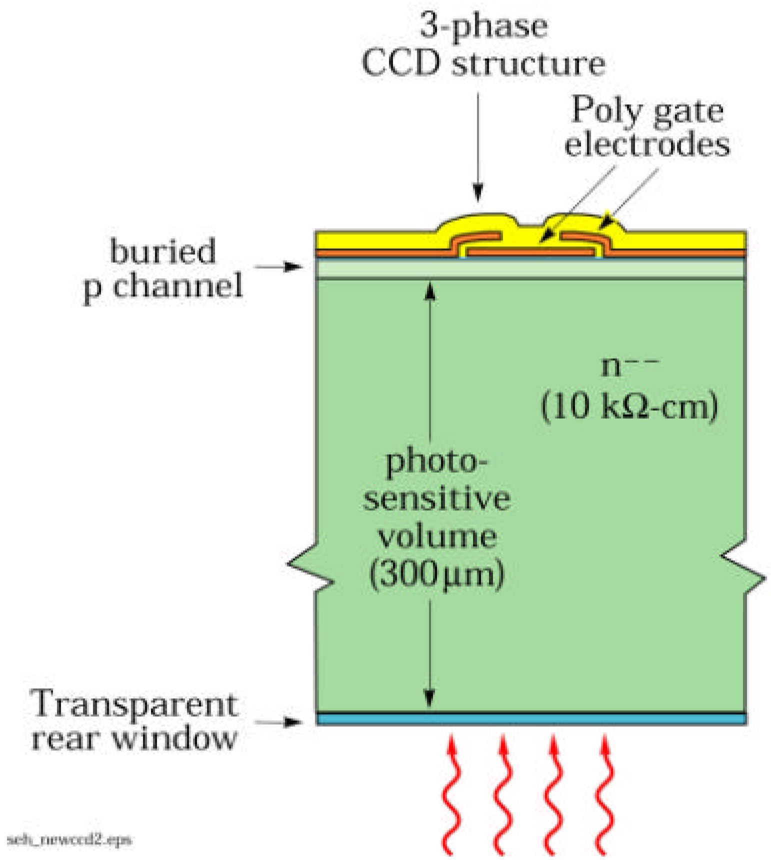
Optical/scanning-electron-microscope photographs taken after poly1 etching





CCD Technology

PROPOSAL:
Make a thick CCD on a high-resistivity n-type substrate, operate fully depleted with rear illumination.



Advantages:

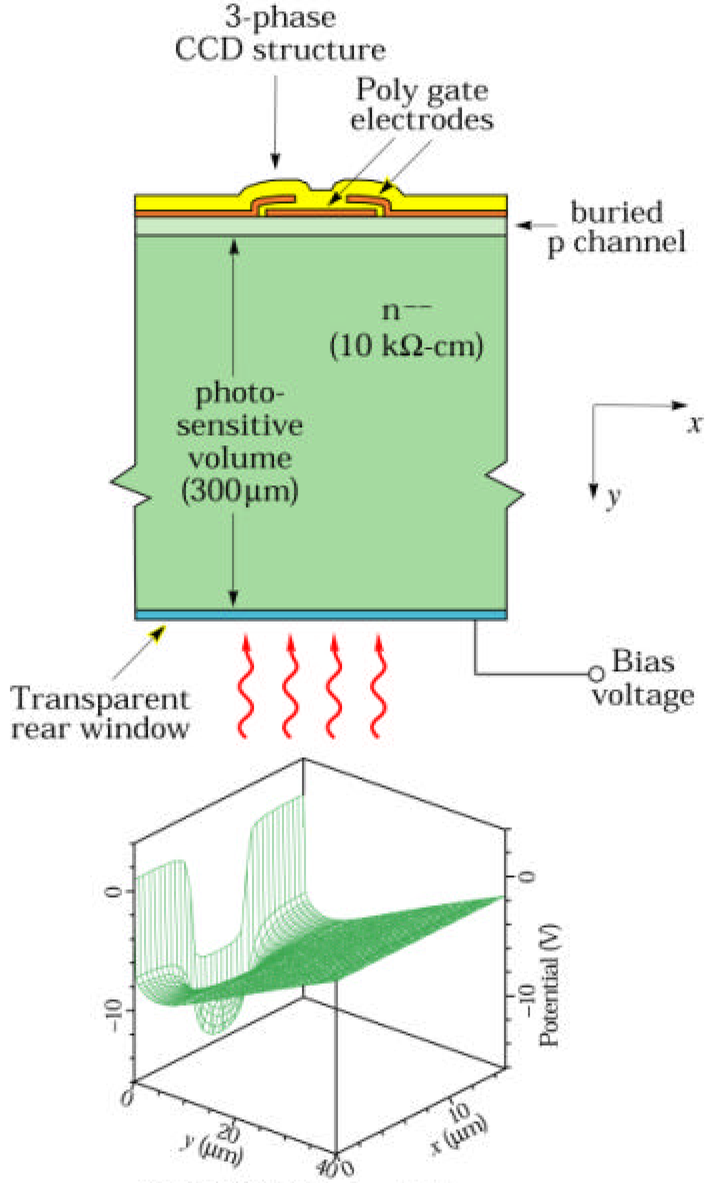
1) Conventional MOS processes with no thinning => "inexpensive"
2) Full quantum efficiency to > 1 µm => no fringing
3) Good blue response with suitably designed rear contact
4) No field-free regions for charge diffusion, good PSF

Disadvantages:

1) Enhanced sensitivity to radiation (x-rays, cosmic rays, radioactive decay)
2) More volume for dark current generation
3) Dislocation generation

CCD Technology

Substrate bias voltage depletes substrate ~ independently of clock voltages



MEDICI 2-D simulation

CCD Technology

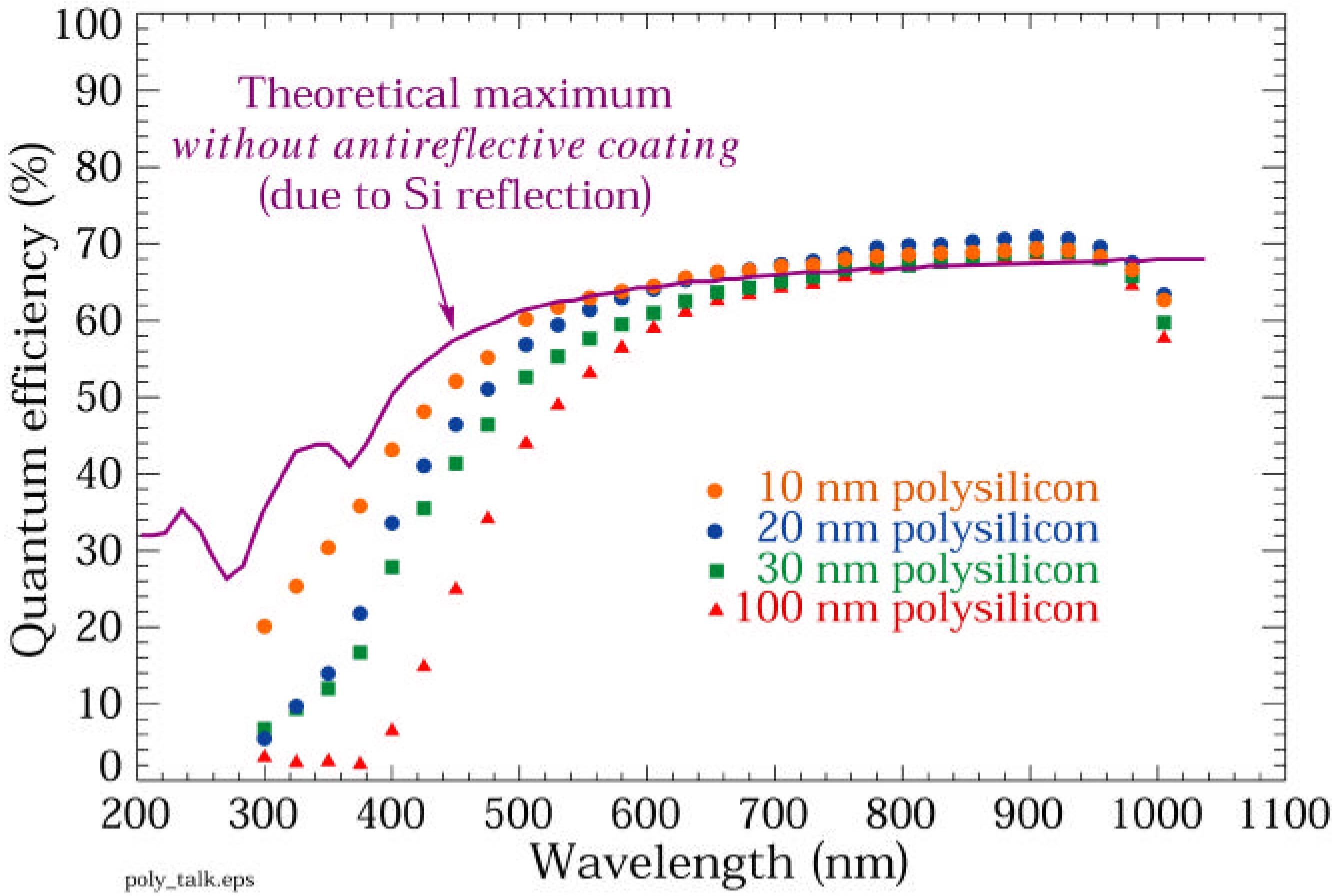
- Conventional CCD fabrication technology with high-resistivity silicon
- Standard processing through the first 8 (of 10) masking steps
- After mask 8 wafers sent out for backgrinding and backside polishing
  - Standard process for thin die applications
- Deposition of thin backside ohmic contact (in-situ doped polysilicon)
  - Back-illuminated photodiode technology licensed to Digirad, Inc for nuclear medical imaging application
- Completion of remaining processing (contact/metal) with 300 μm thick wafer, requiring focus adjustment of lithography equipment at foundry (standard is 500-600 μm)
- Deposition of antireflection coatings on wafer backside

Successful fabrication of 100 mm front-illuminated control CCD and 150 mm photodiode wafers at commercial foundry

LBNL completion of wafers processed through mask 8 by commercial foundry in progress

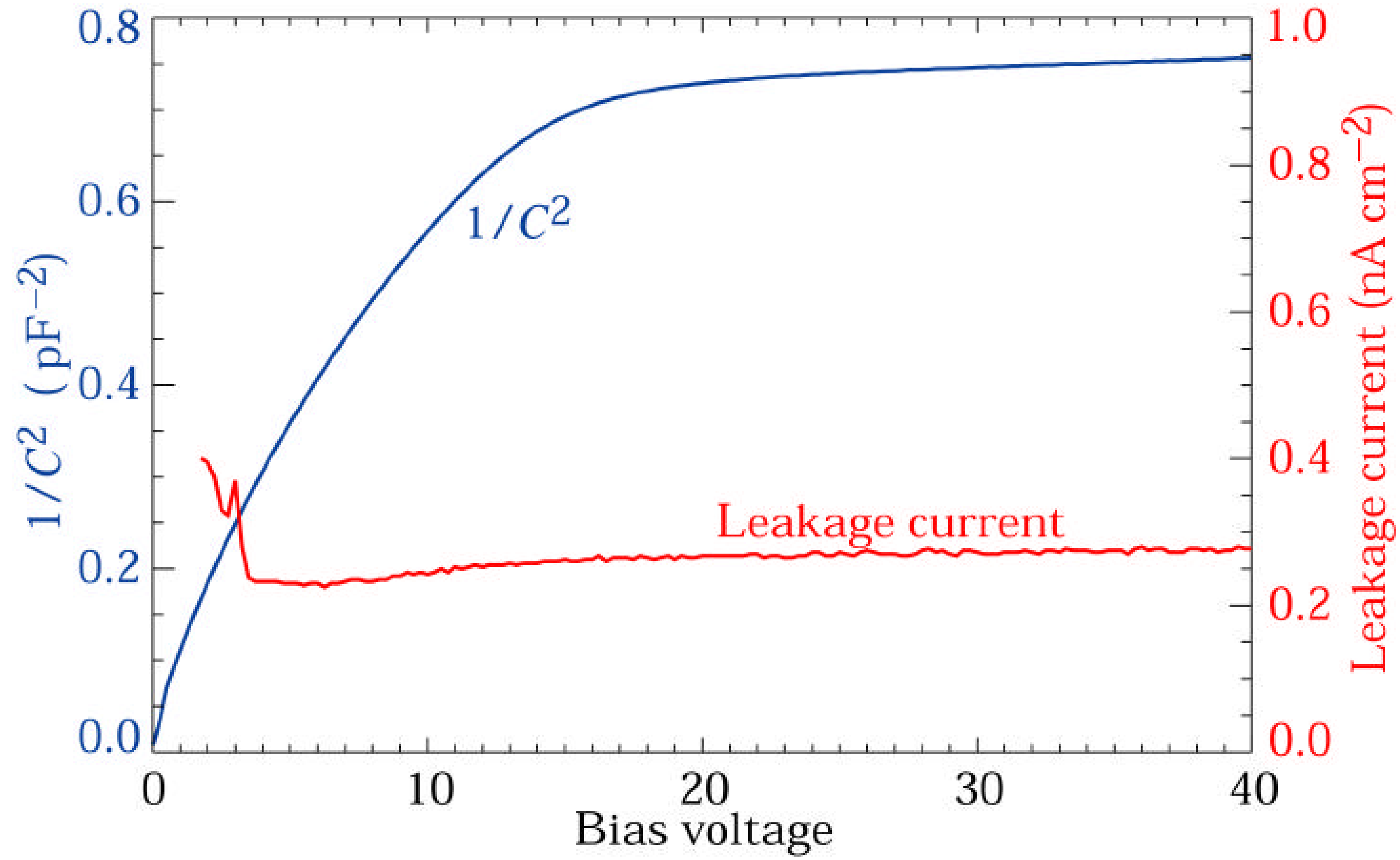
Transparent back-side contact technology

Back-illuminated photodiodes

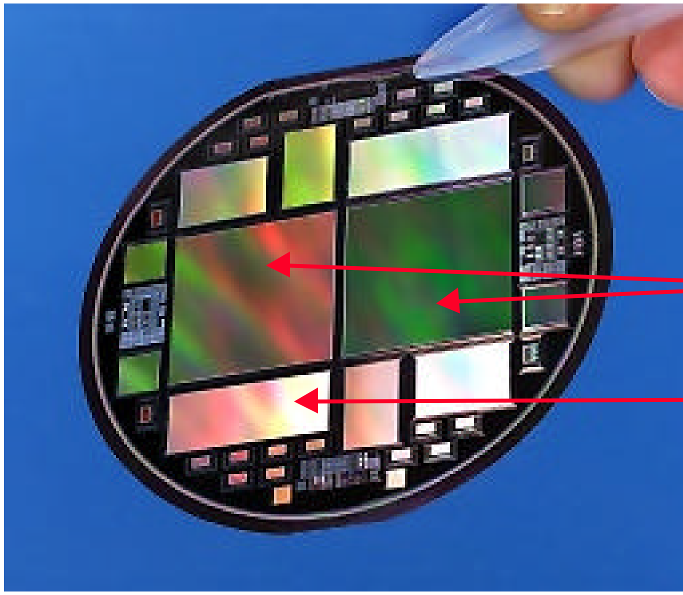


Transparent back-side contact technology

p-i-n test device on back-illuminated CCD wafer



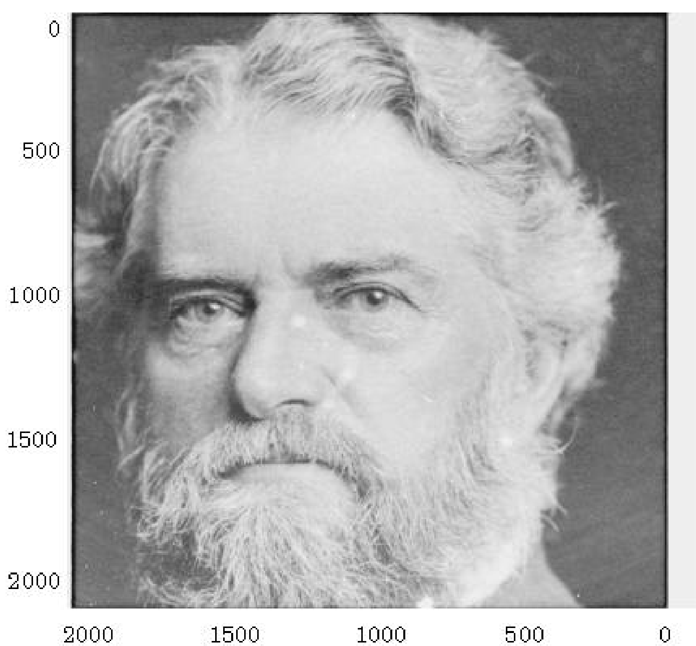
LBNL 2k x 2k

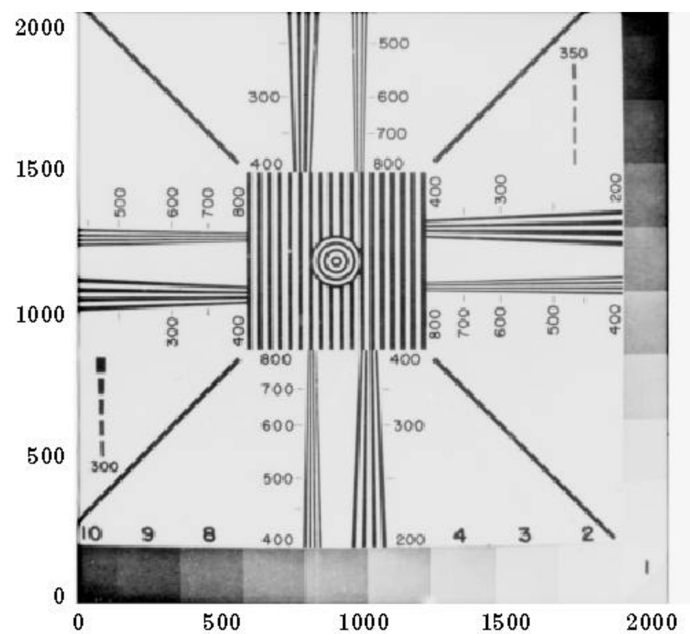


First large format CCD made at LBNL

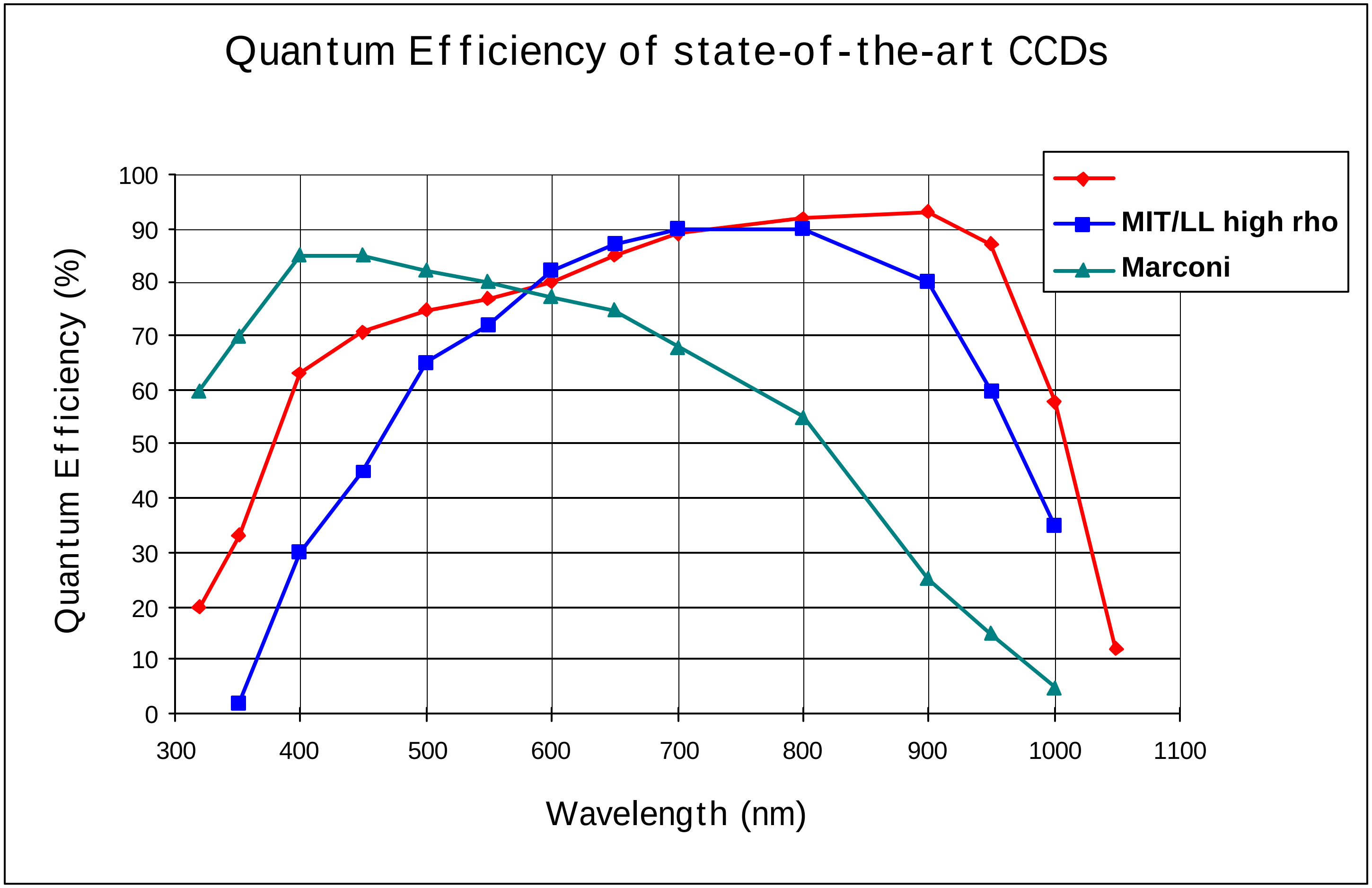
2k x 2k, 15 μm pixels.

1980 x 800, 15 μm pixels.





LBNL 2k x 2k QE



From "An assessment of the optical detector systems of the W.M. Keck Observatory," J. Beletic, R. Stover, K Taylor, 19 January 2001.

LBNL 2k x 2k results

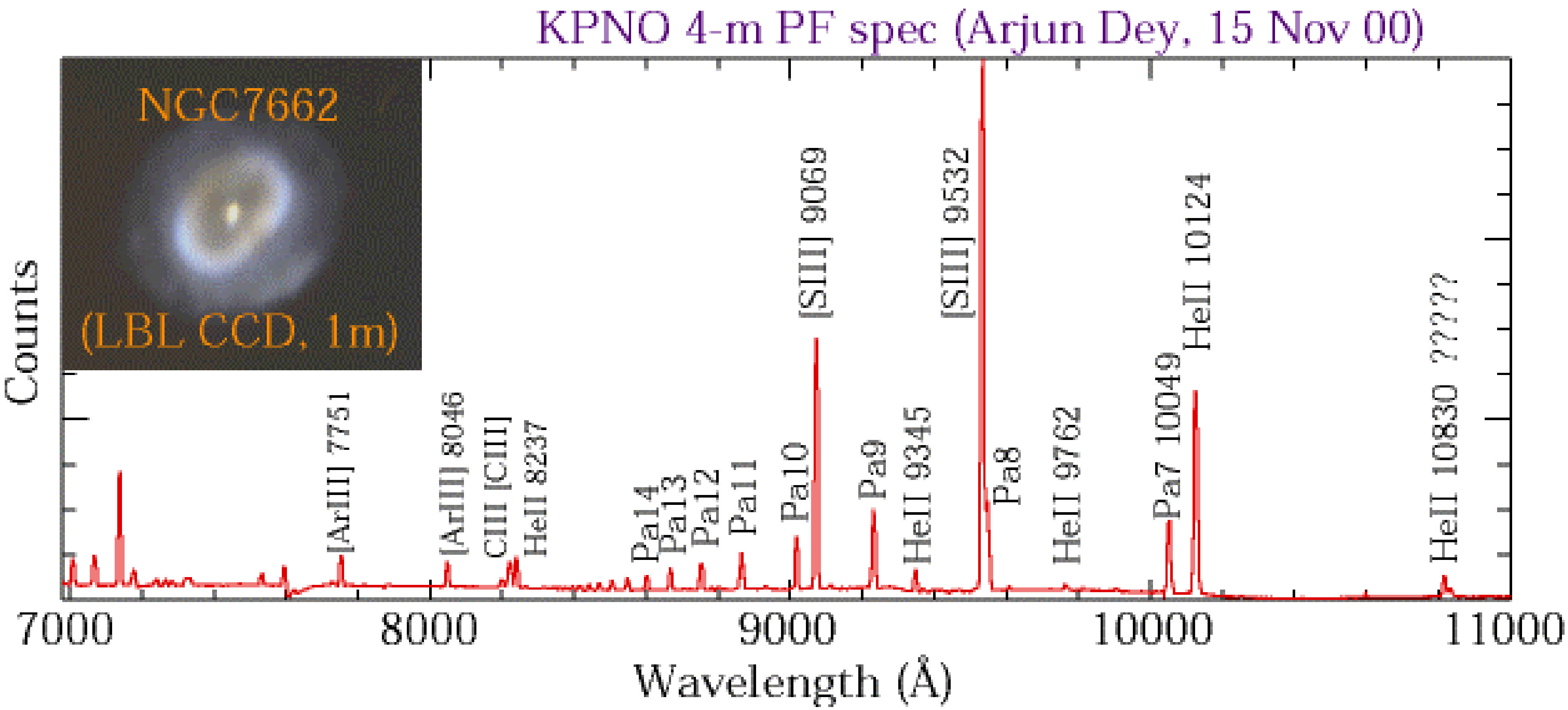
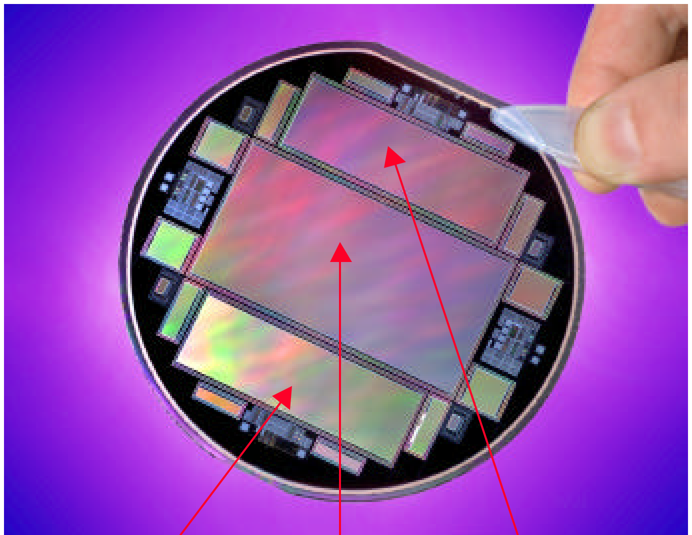


Image: 200 x 200 15 mm LBNL CCD in Lick Nickel 1m.
Spectrum: 800 x 1980 15 mm LBNL CCD in NOAO KPNO spectrograph.
Instrument at NOAO KPNO 2nd semester 2001 (http://www.noao.edu)

LBNL 2k x 4k



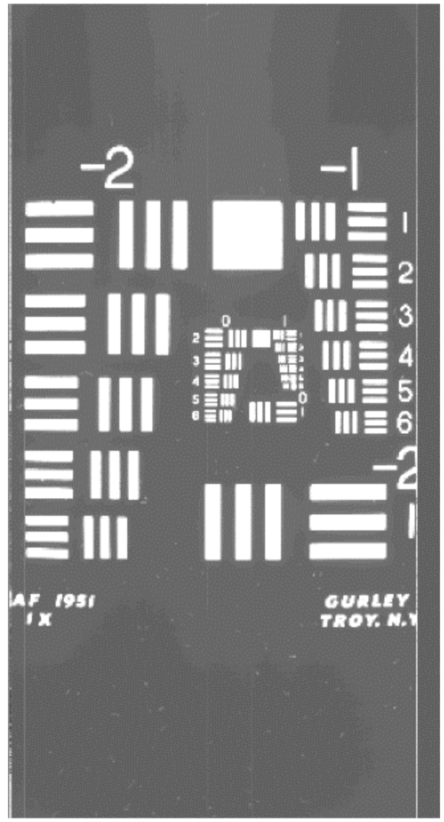
1478 x 4784
10.5 mm

2k x 4k
15 mm

1294 x 4186
12 mm

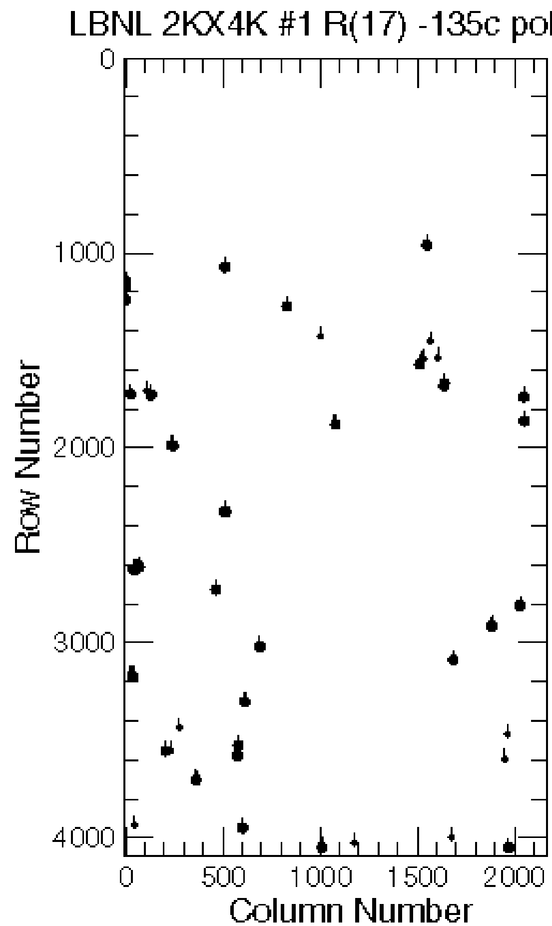
USAF test pattern.

LBNL 2KX4K #1 R(17) -135c image

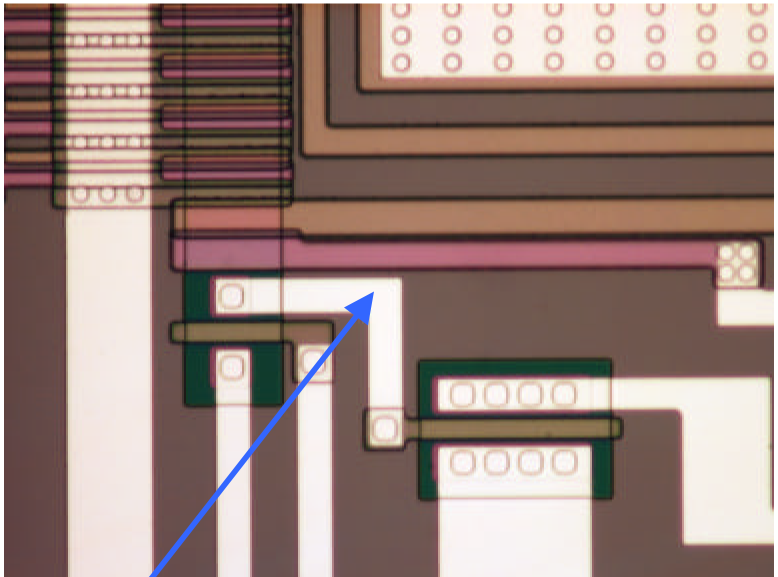


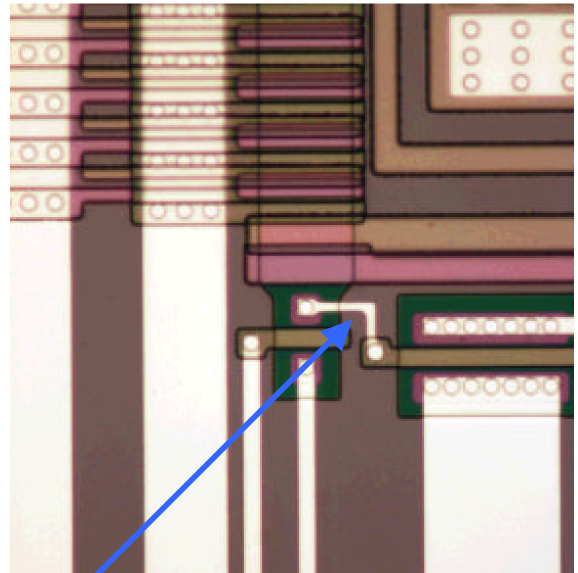
Size: 512 Rows, 272 Cols Origin (0,0)

Trap sites found by pocket pumping.



Amplifier noise studies



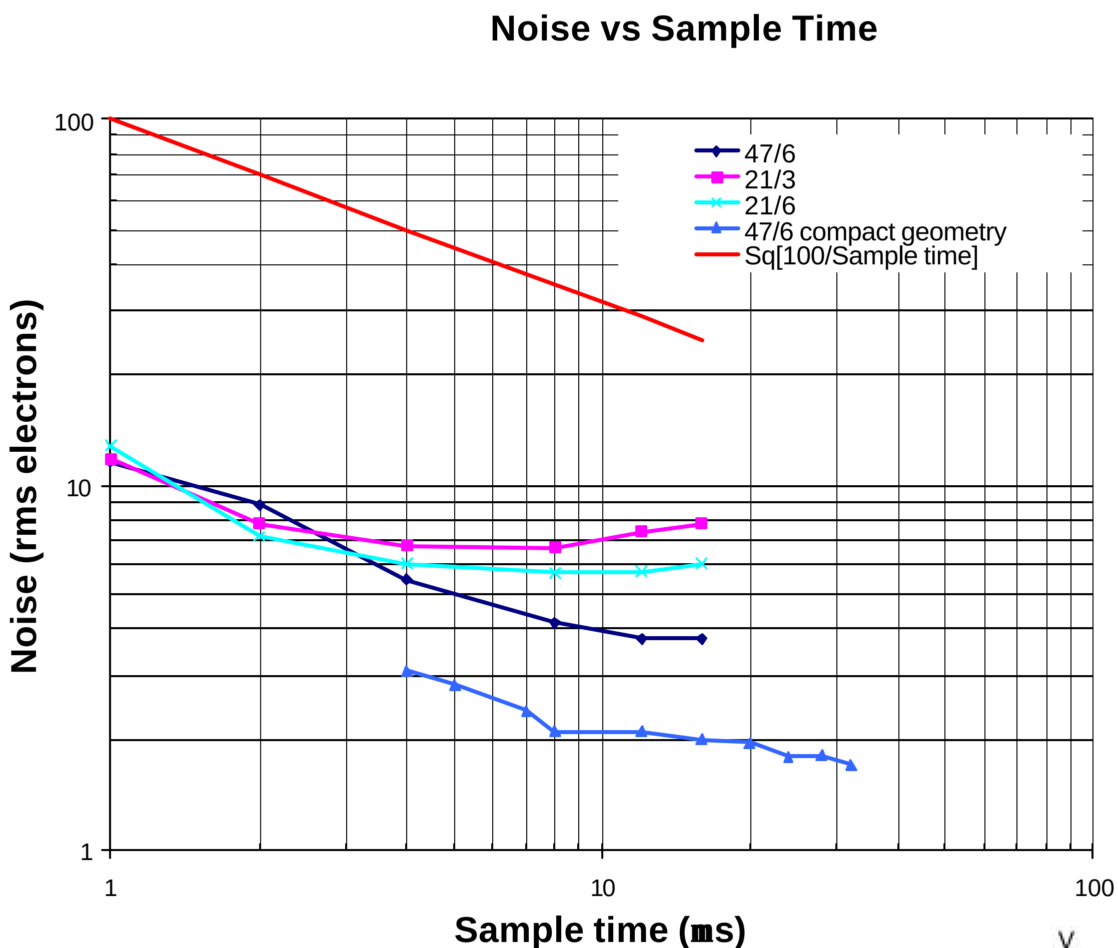


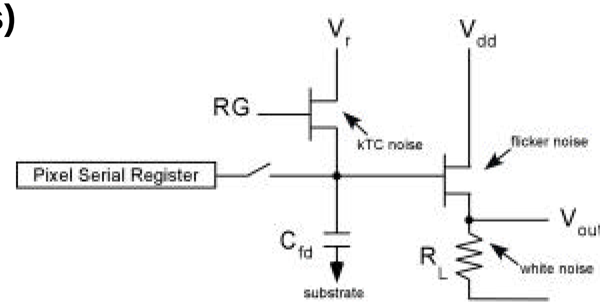
“Standard” amplifier connection between floating diffusion and output source follower transistor

Revised version with more aggressive design rules

Read Noise Measurements

Noise after correlated double sampling.

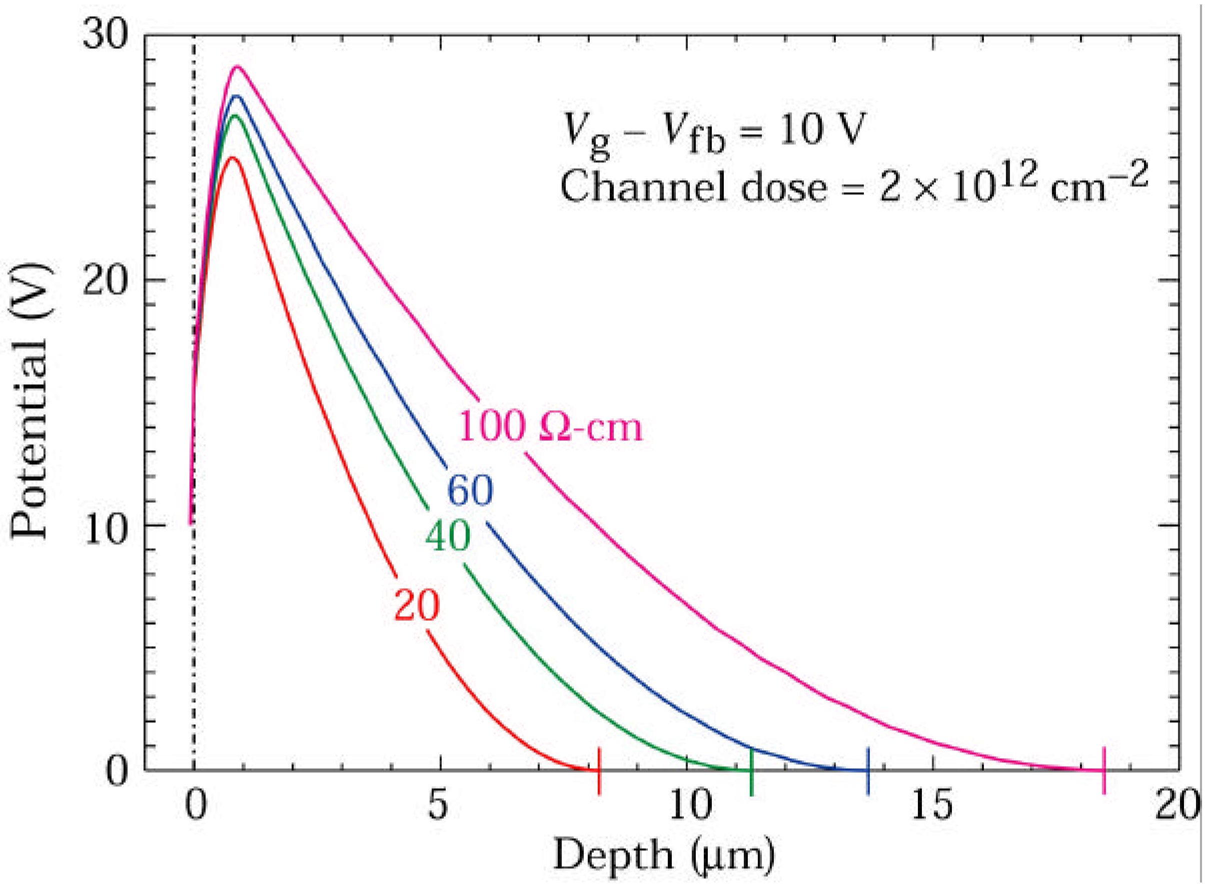




Sample time is the width of the reset or video integration.

Point Spread Function Issues

Low-resistivity CCD (typically 20 μm thick): PSF dominated by carrier diffusion in field-free regions. σ = Thickness of field-free region.



Calculated CCD potential versus depth

Point Spread Function Issues

- Fully depleted CCD: PSF determined by hole transit time in electric field
- For carriers with the same arrival time at the CCD potential wells, the distribution is Gaussian

Constant field approximation

$$s = \sqrt{2D_p t_{tr}} \qquad t_{tr} = \frac{z_{sub}}{v} = \frac{z_{sub}}{m_p E} = \frac{z_{sub}^{\;2}}{m_p (V_{sub} - V_J)}$$

$$D_p / m_p = kT / q \qquad \boxed{s = z_{sub}\sqrt{\frac{kT}{q}\frac{2}{(V_{sub} - V_J)}}}$$

z_{sub} ~ Thickness of CCD

kT / q Thermal voltage

$V_{sub} - V_J$ Voltage across drift region

PSF Measurements at Lick Observatory

Hamilton Coude Echelle Spectrograph
FWHM from Calibration Lamp Spectra

All CCDs have 15 µm pixels

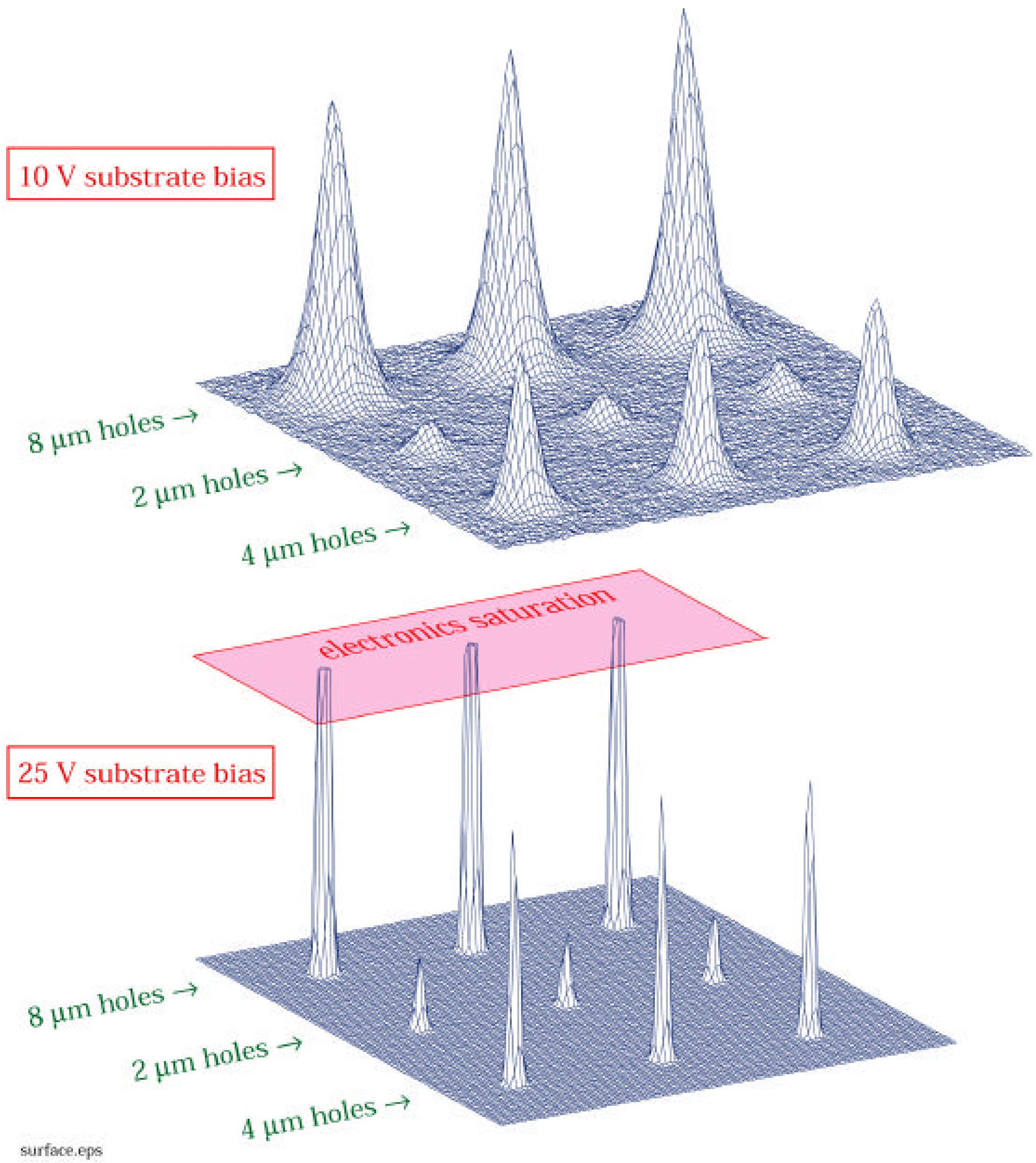
Device	*FWHM (pixels)*	*Notes*
Loral Frontside	1.25	
Loral Thinned/Backside	1.90	
LBNL Backside (300 µm)	1.95	40V subr. bias
LBNL Backside (200 µm)	1.60	40V subr. bias

$$\frac{\sqrt{1.60^2 - 1.25^2}}{\sqrt{1.95^2 - 1.25^2}} \approx 0.67$$

$$s \approx 6.4/9.6mm(200/300mm)_{V_{sub}=40V}$$

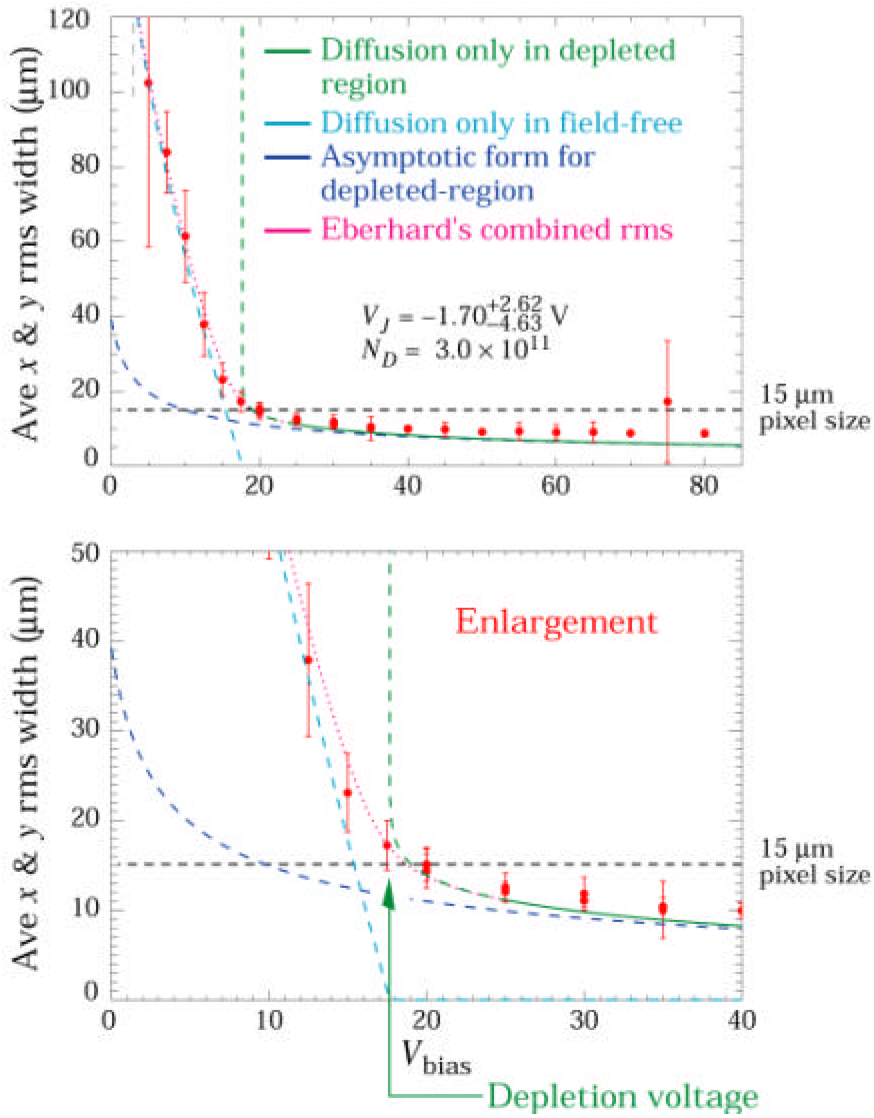
Consistent with pinhole mask/cosmic ray experiments

Measurement of PSF with pinhole mask



Measurement of PSF with pinhole mask

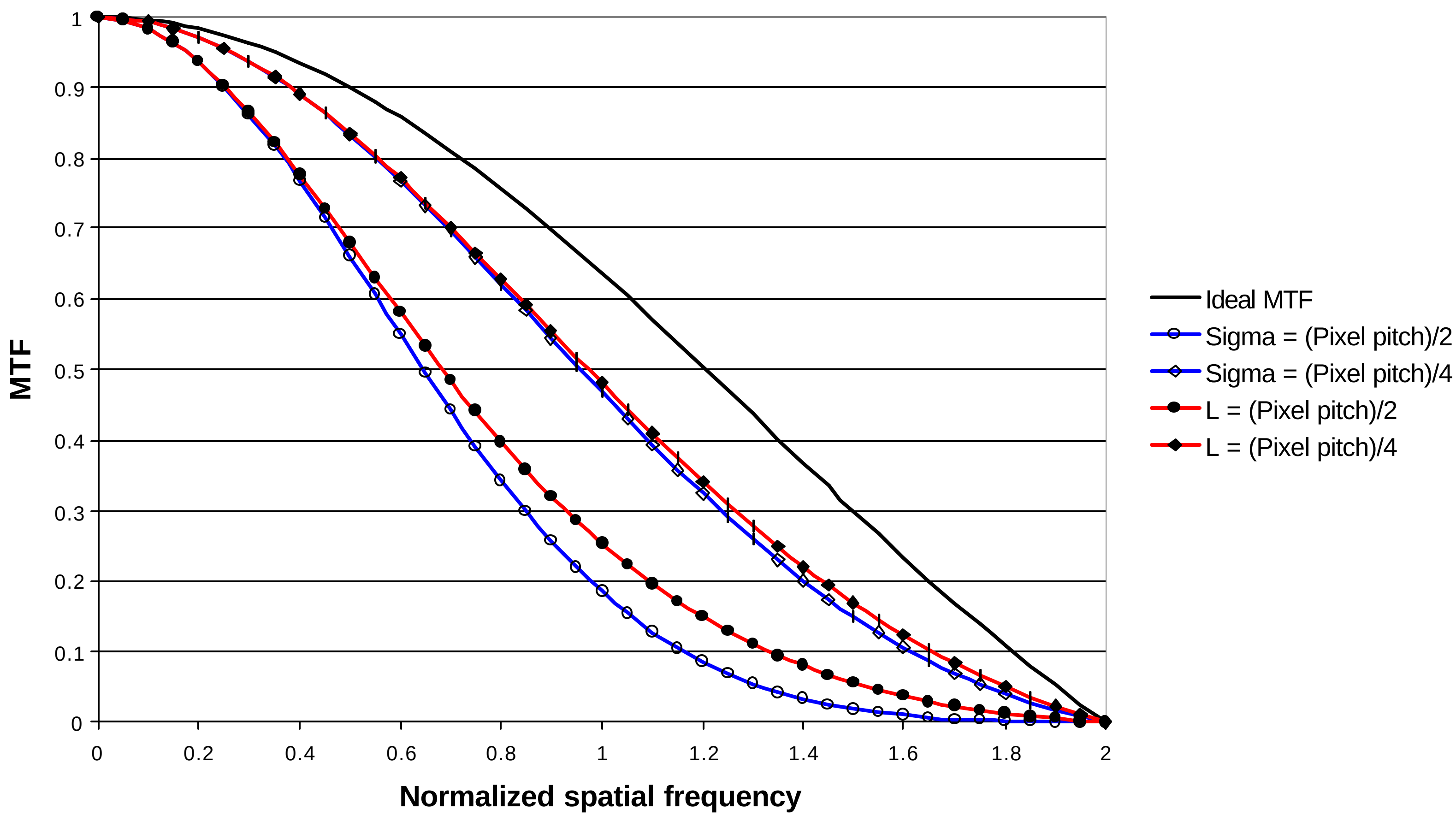
Measurements at Lick Observatory



Modulation Transfer Function

Theoretical MTF calculations

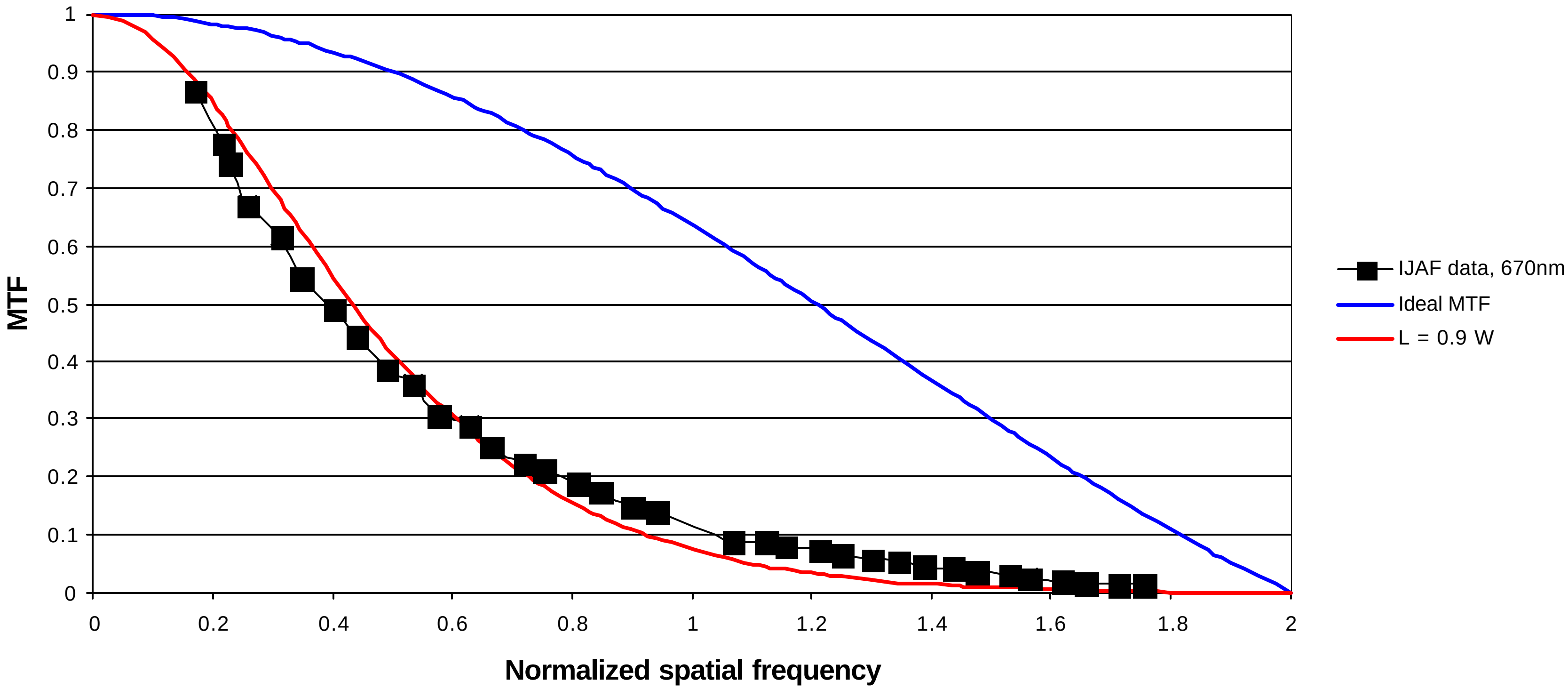
Ideal MTF convolved with /



Thinned CCD MTF Data

Data from Nordic Optical Telescope

Loral CCD thinned at University of Arizona



Commercialization efforts

- Started with CCD effort on 100 mm wafer processing line
- Front-illuminated high-resistivity CCD's were successfully produced
- Processing to mask layer 8 at foundry with completion of processing at LBNL in progress (back illuminated)
- Similar effort at the foundry failed due to processing error

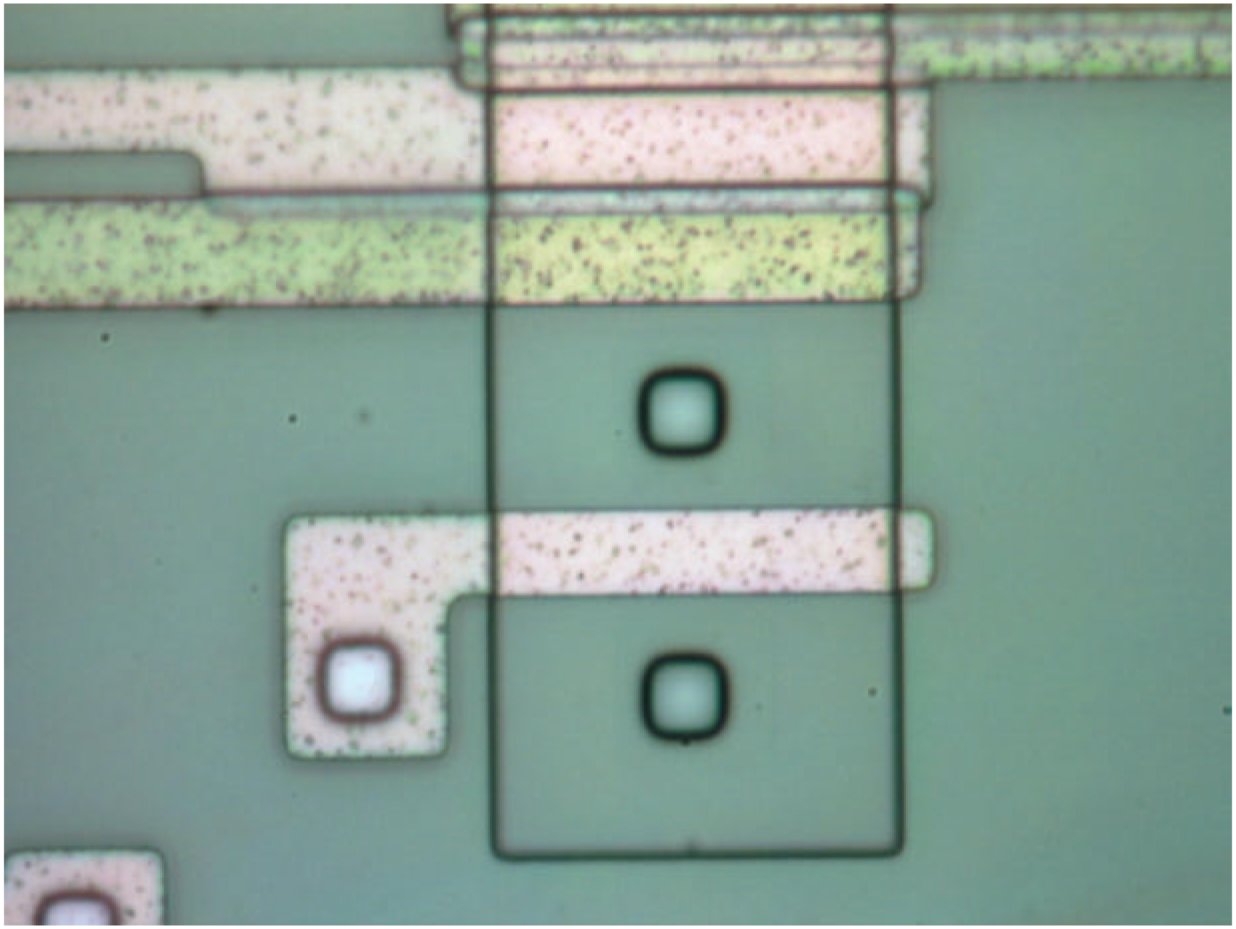
- Downsizing of 100 mm line forces change to 150 mm line
- First lot consists of photodiode arrays
  — Simpler process although major high-temperature steps are included
  — Straightforward to test arrays for dark current uniformity
  — First attempt at backgrinding and thinning of 150 mm wafers

- First 150 mm CCD lot will not be thinned for rapid turnaround
  — Lot starts week of March 19^{th}, 9-11 week turnaround

- Second 150 mm lot using same mask set will be processed for back illumination

CCD Technology

CCD fabricated at commercial foundry through mask 8, contact etching and remaining processing performed at LBNL (in progress)



LBNL back end processing no longer viable with switch to 150 mm wafers

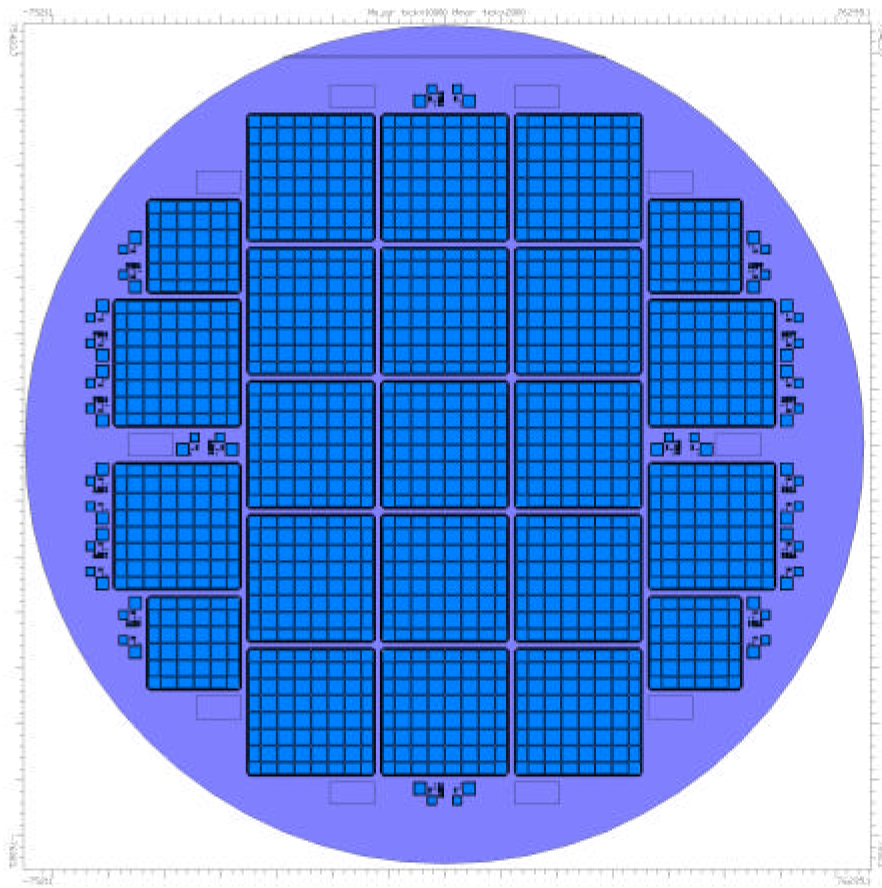
Commercial PIN Diodes

150 mm mask layout for 8 x 8 (3 mm x 3 mm pixel) PIN diode arrays.

First wafers delivered late Feb 2001.

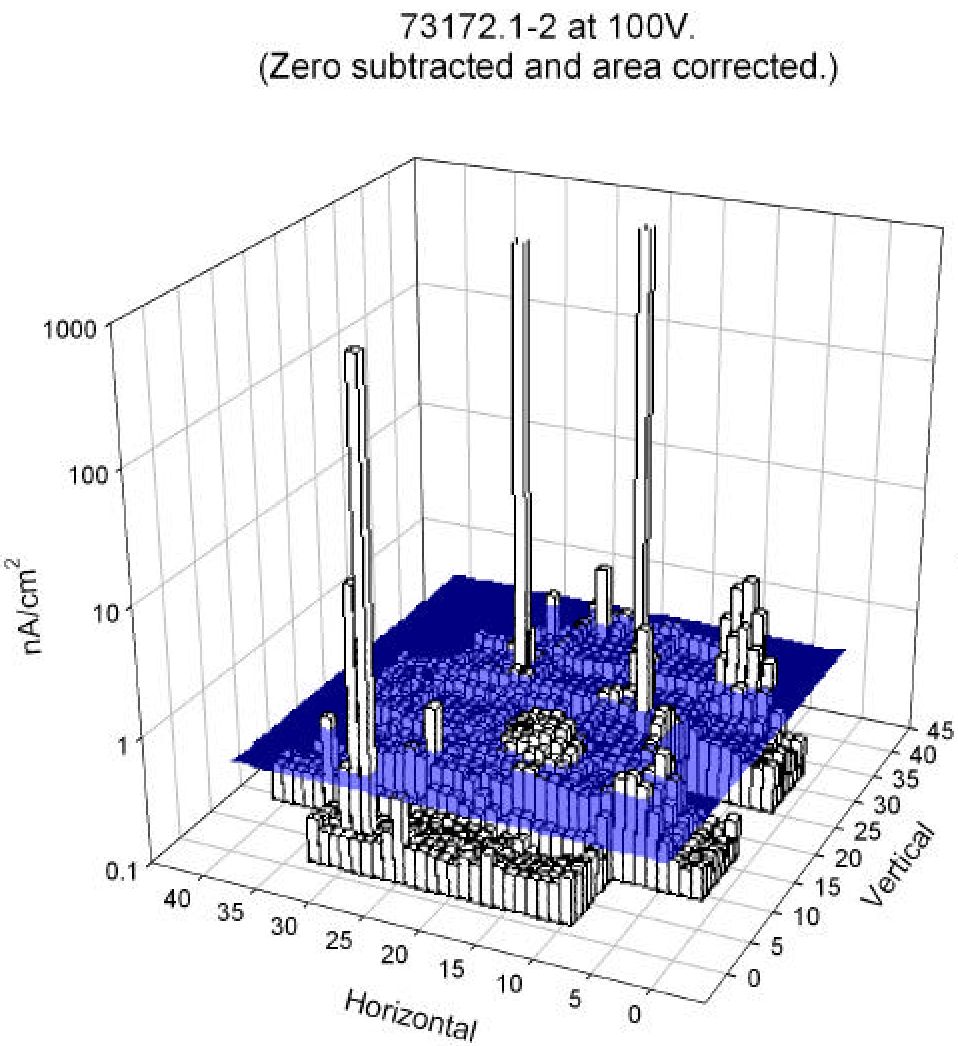
Excellent dark current uniformity measured on control wafers. Pixel yield > 98%, 2-3 killer defects per wafer.

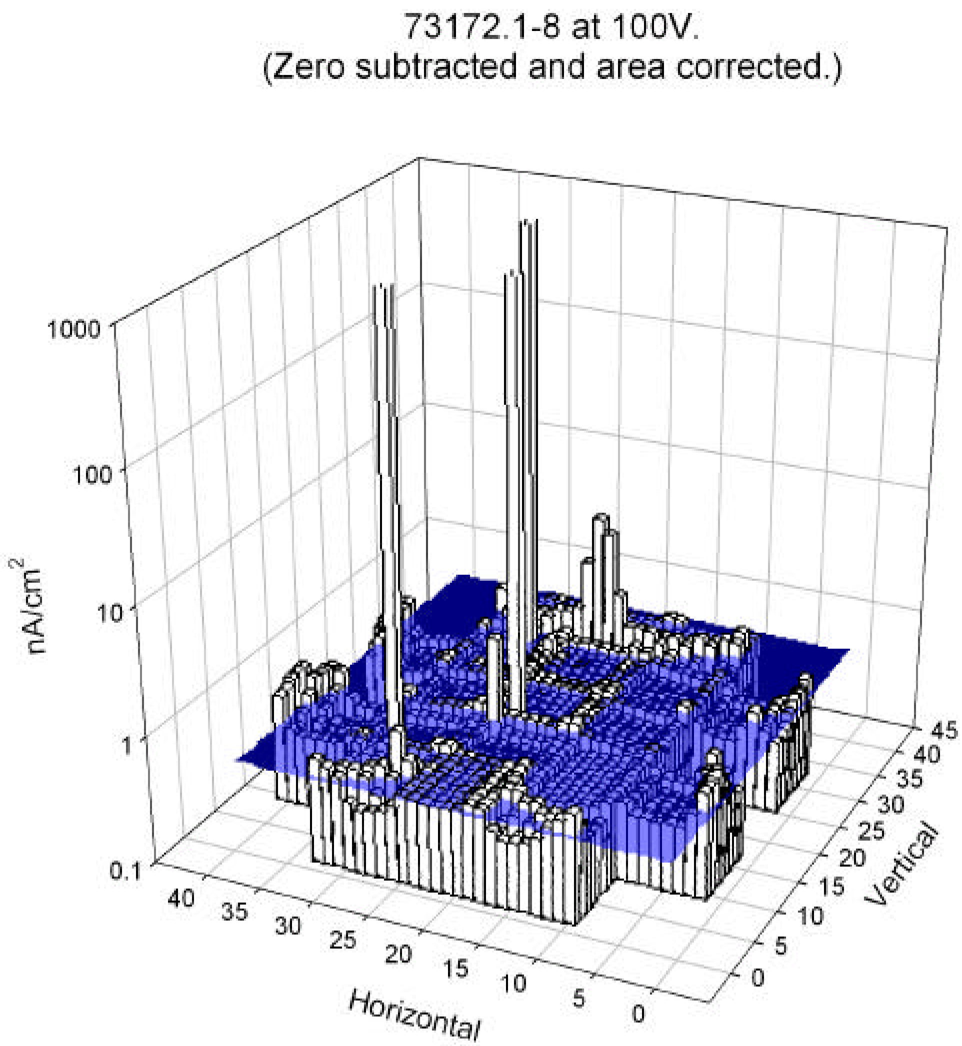
First back-illuminated wafers in progress (300, 360 μm).



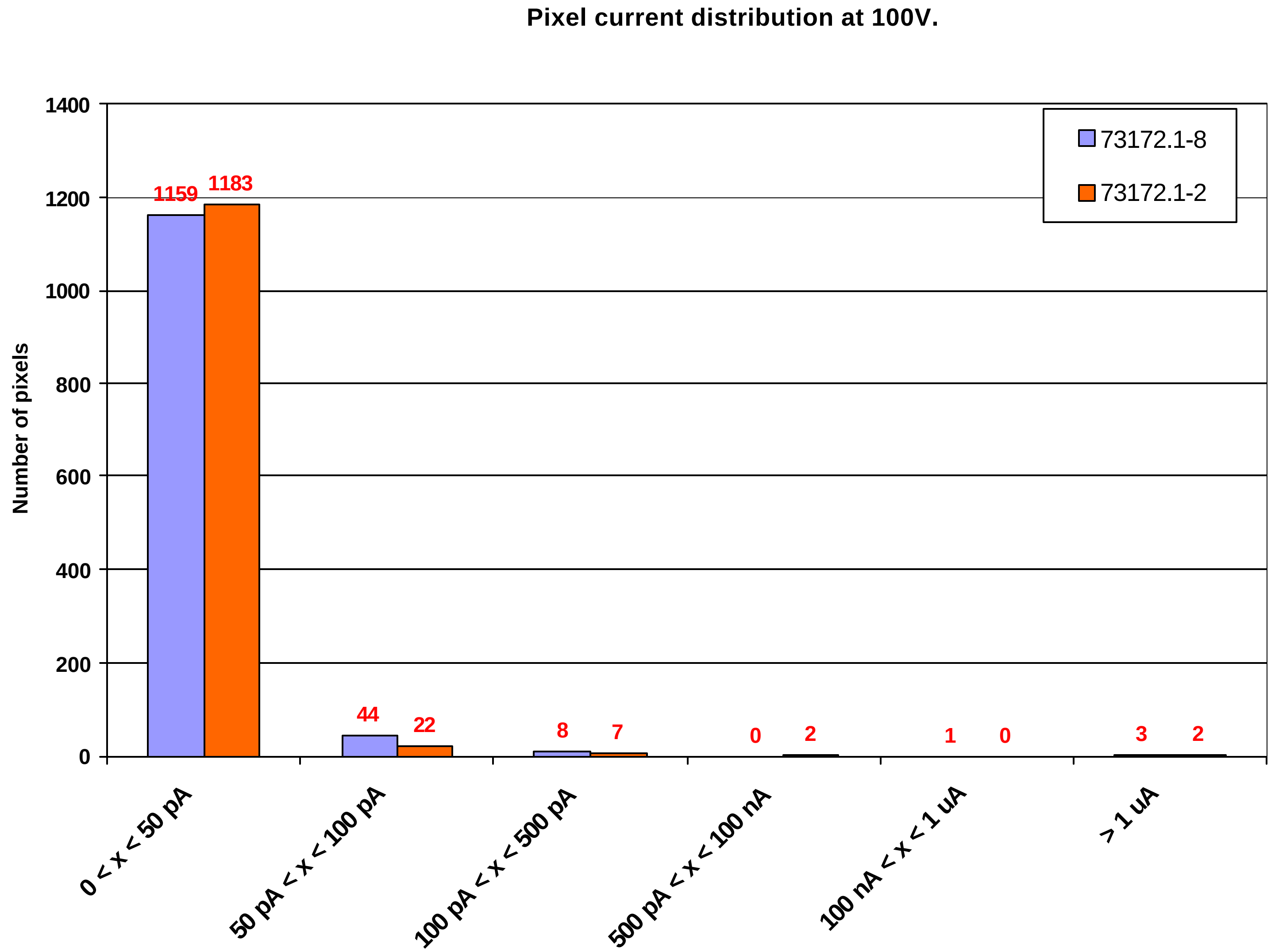
Dark current measurements on 150 mm wafers

Cloud level is at 0.5 nA/cm^2





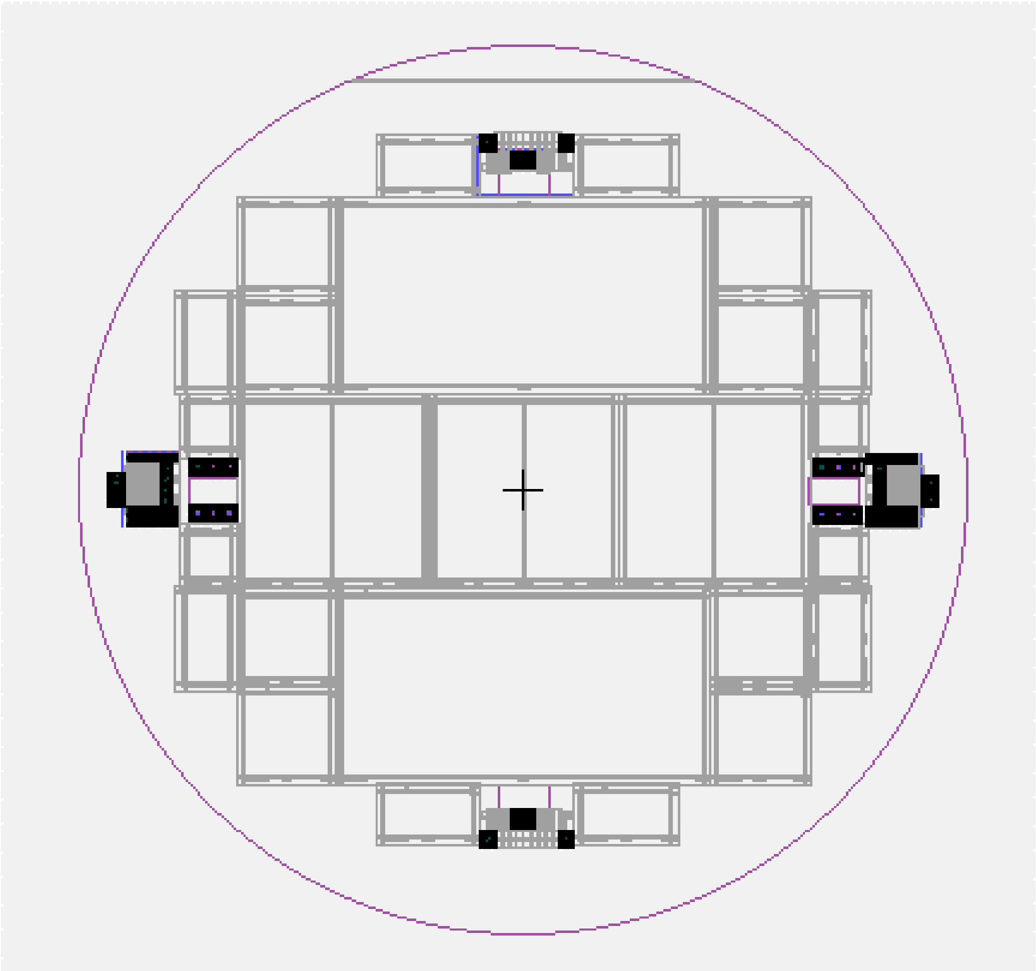
Dark current distribution



150 mm CCD layout

Includes

- 982 x 935 (15 μm)^2
- 1230 x 1170 (12 μm)^2
- 1402 x 1336 (10.5 μm)^2
- 1636 x 1560 (9 μm)^2
- 2520^2 (12 μm)^2
- 2880^2 (10.5 μm)^2
- 2048 x 4096 (15 μm)^2
- 512^2 & 1024 x 512 (15 μm)^2
  Amplifier studies (noise)
- 1200 x 600 (15 μm)^2
  2-stage amplifiers for
  high-speed readout



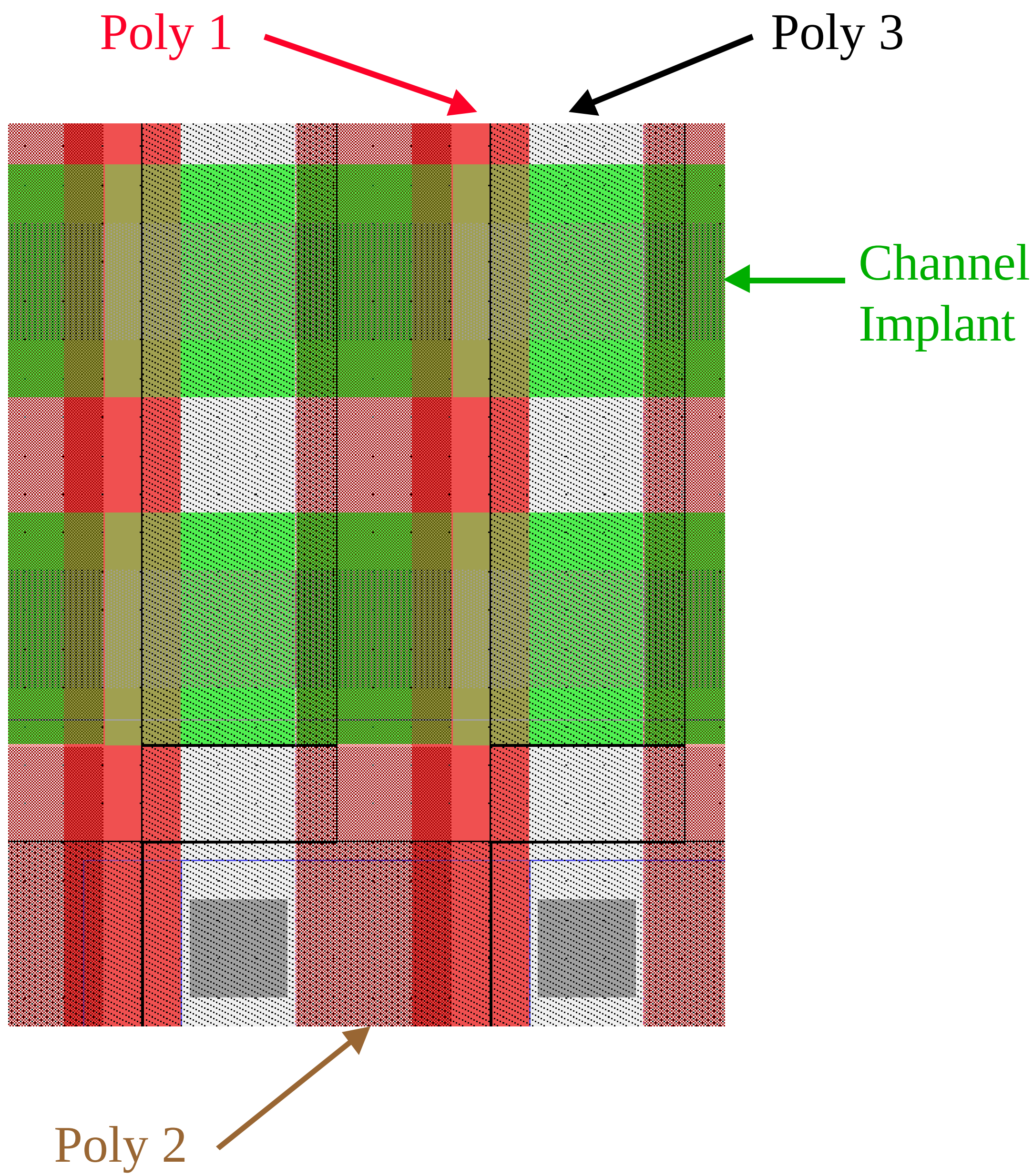
9 mm pixel issues

Poly 2 and 3 overlap of Poly 1 leaves 1 μm gap between Poly 2 and 3. Step coverage concern for misalignment resulting in triple poly overlap.

Channel area only 22.5% of 15 μm pixel due to losses from channel stop (3 μm) and super notch.

Resulting reduced full well could limit readout speed due to lack of fringing fields near full well.

MTF concerns.



Two-stage amplifier studies

Source follower bandwidth

$$f_{-3db} = \frac{1}{2p}\frac{g_m}{C_{load}}$$

Typical design number C_{load} ~ 10 pF
LBNL standard output transistor g_m ~ 150 μA/V
Maximum bandwidth ~ 2.4 MHz

$$g_m \propto \sqrt{\frac{W}{L} I_{DS}}$$

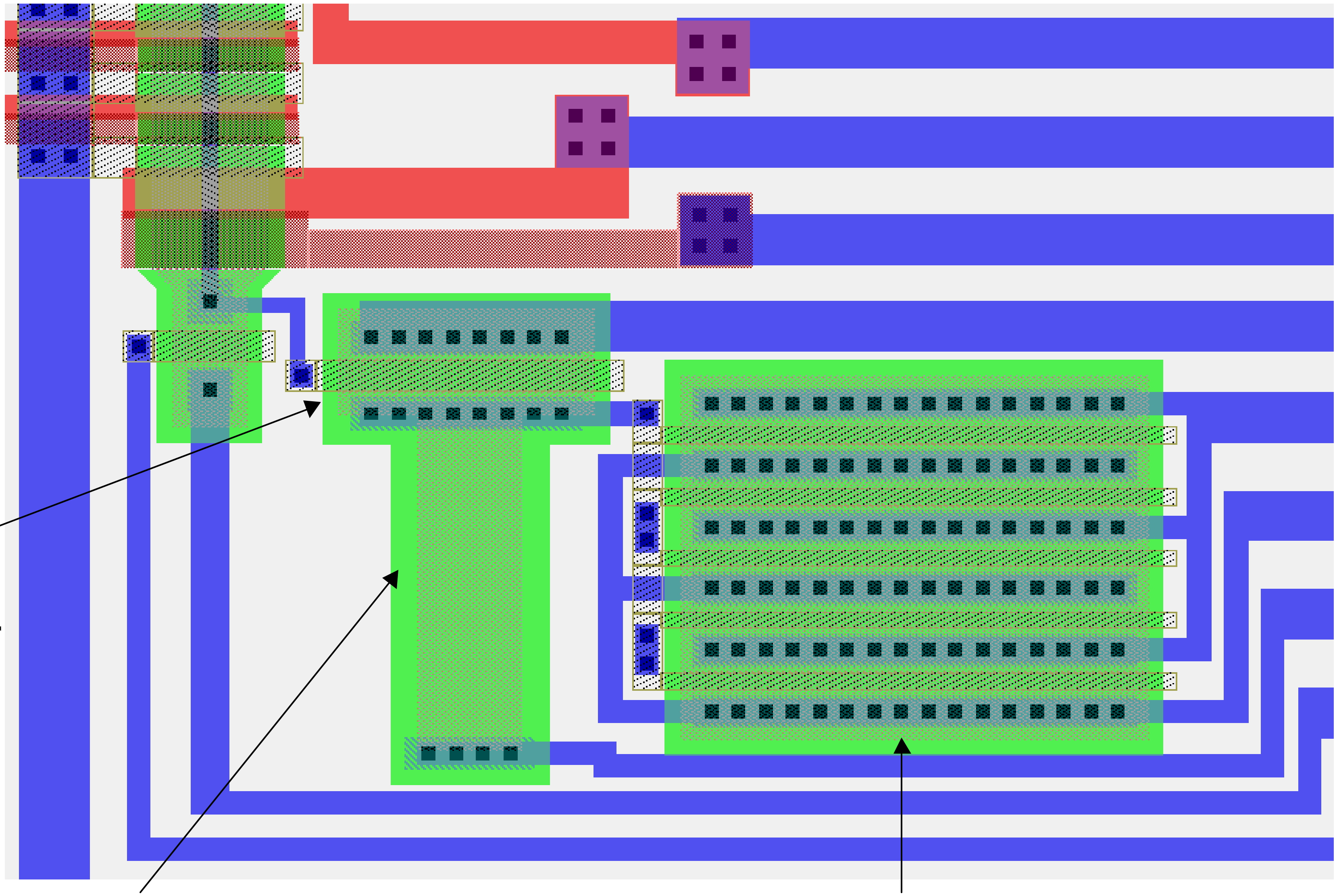
Keep standard 47/6 1st stage transistor for low noise, add 2nd stage to drive output. 450/3 output transistor should drive 10 pF at 10MHz with some design margin.

Two-stage amplifier load devices

- Channel-implant resistor
  - Low noise
  - Large temperature coefficient due to temperature dependence of hole mobility
  - JFET-type behavior (pinchoff)
- Poly resistor
  - No high value poly resistor in foundry CCD process
  - Enough room for a gate-poly resistor
  - Requires minimum design rule width, sensitive to process variations
- Transistor
  - Glow concerns for transistor driven deep into saturation
  - Gate and source brought out to pads, separate V_{dd} for each stage
- External resistor
  - Require < 2.4 pF for 10MHz operation

All the above implemented on 1200 x 600 (15 μm pixel) CCD's as well as on individual amplifier test structures (150 mm wafer layout)

Channel-implant resistor

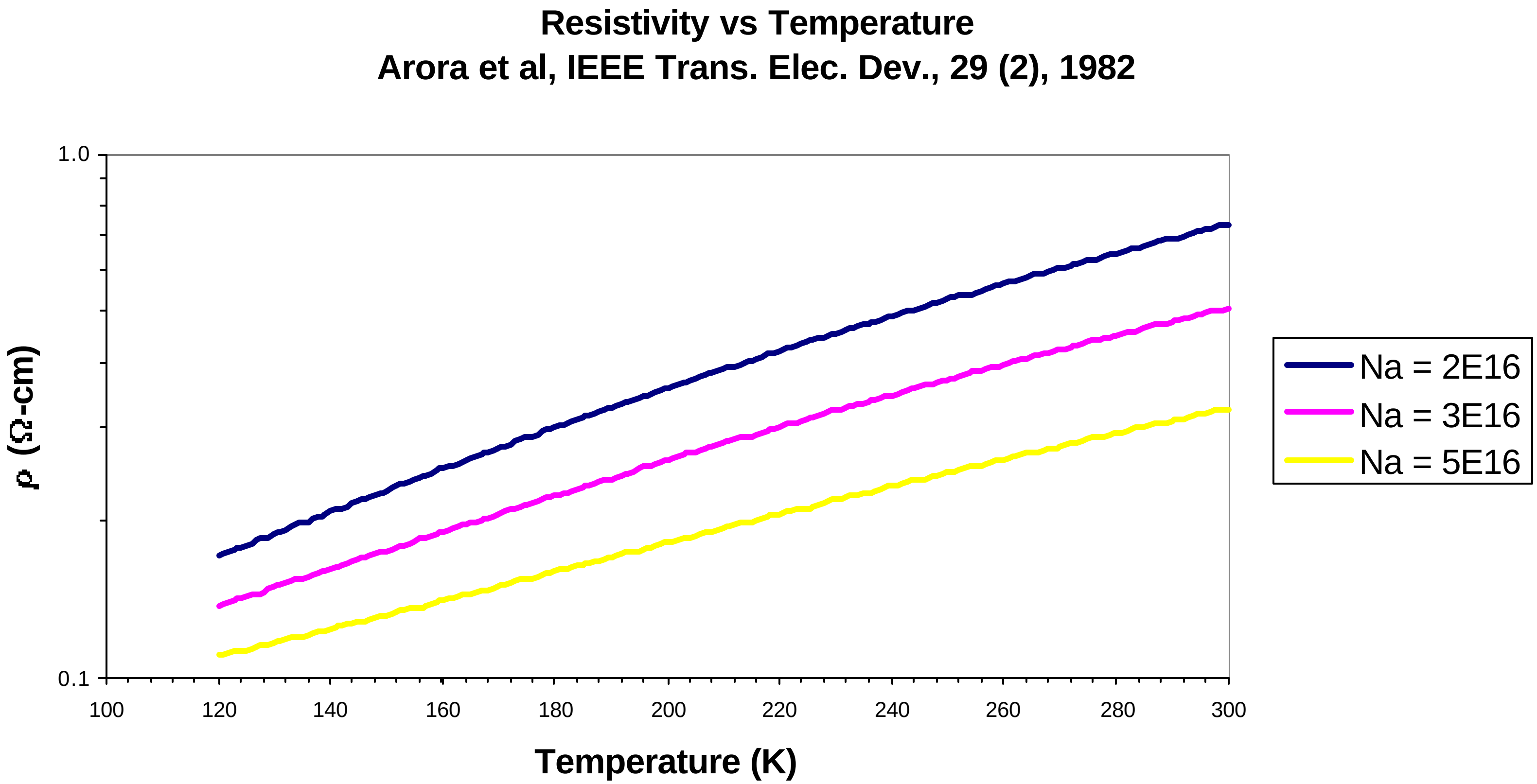


47/6
1st stage
transistor

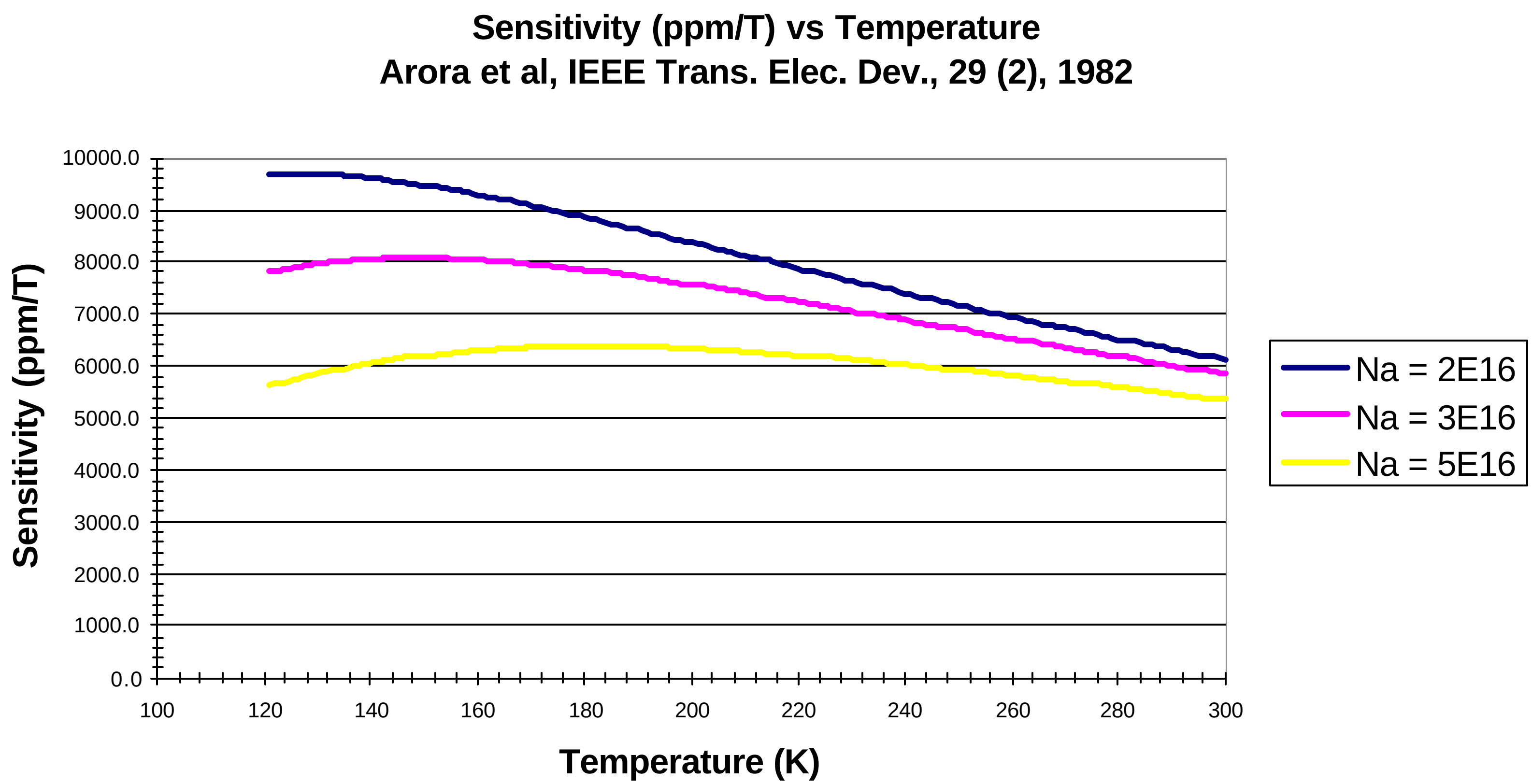
Channel-implant resistor

450/3 output transistor

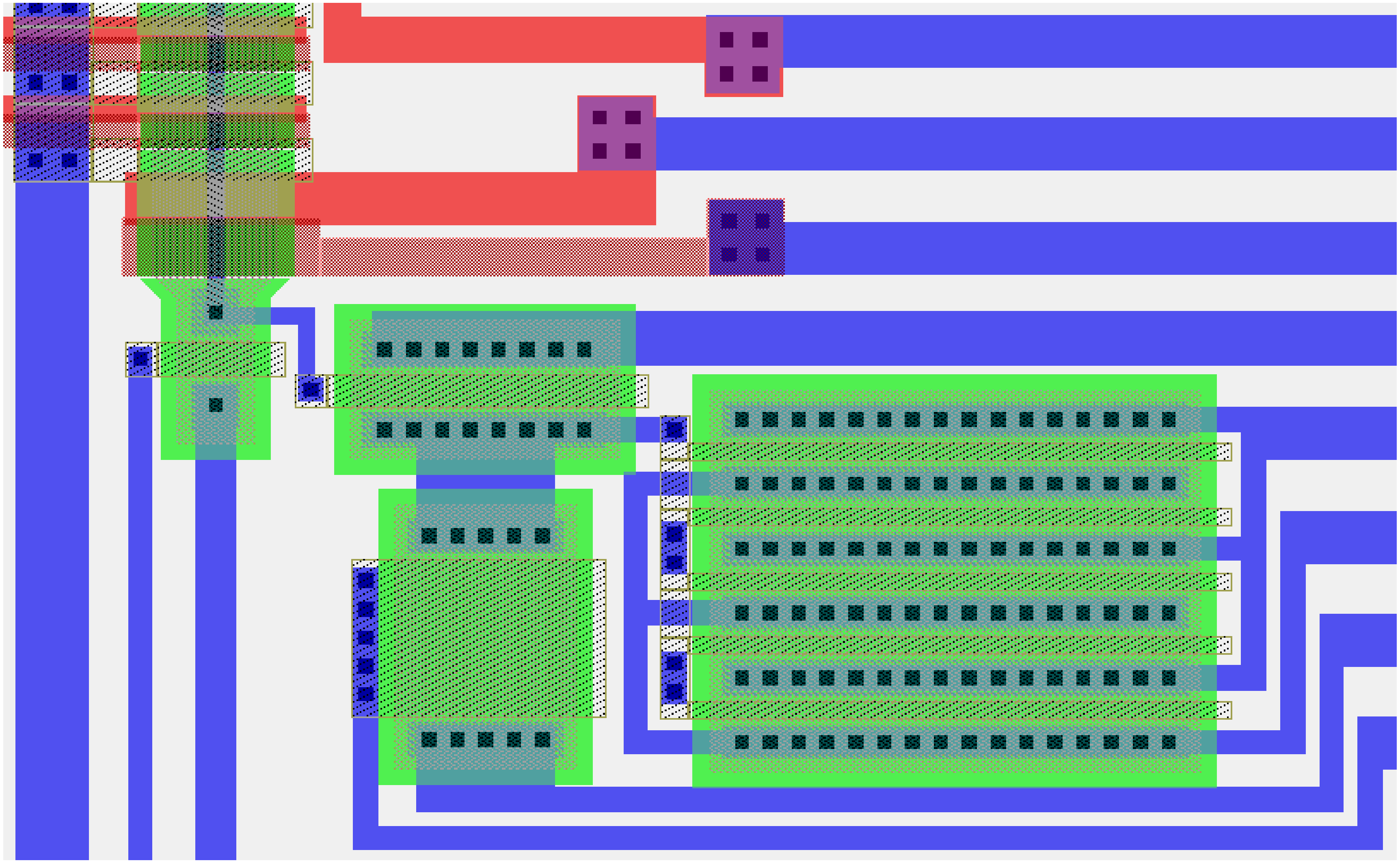
Channel-resistor temperature dependence



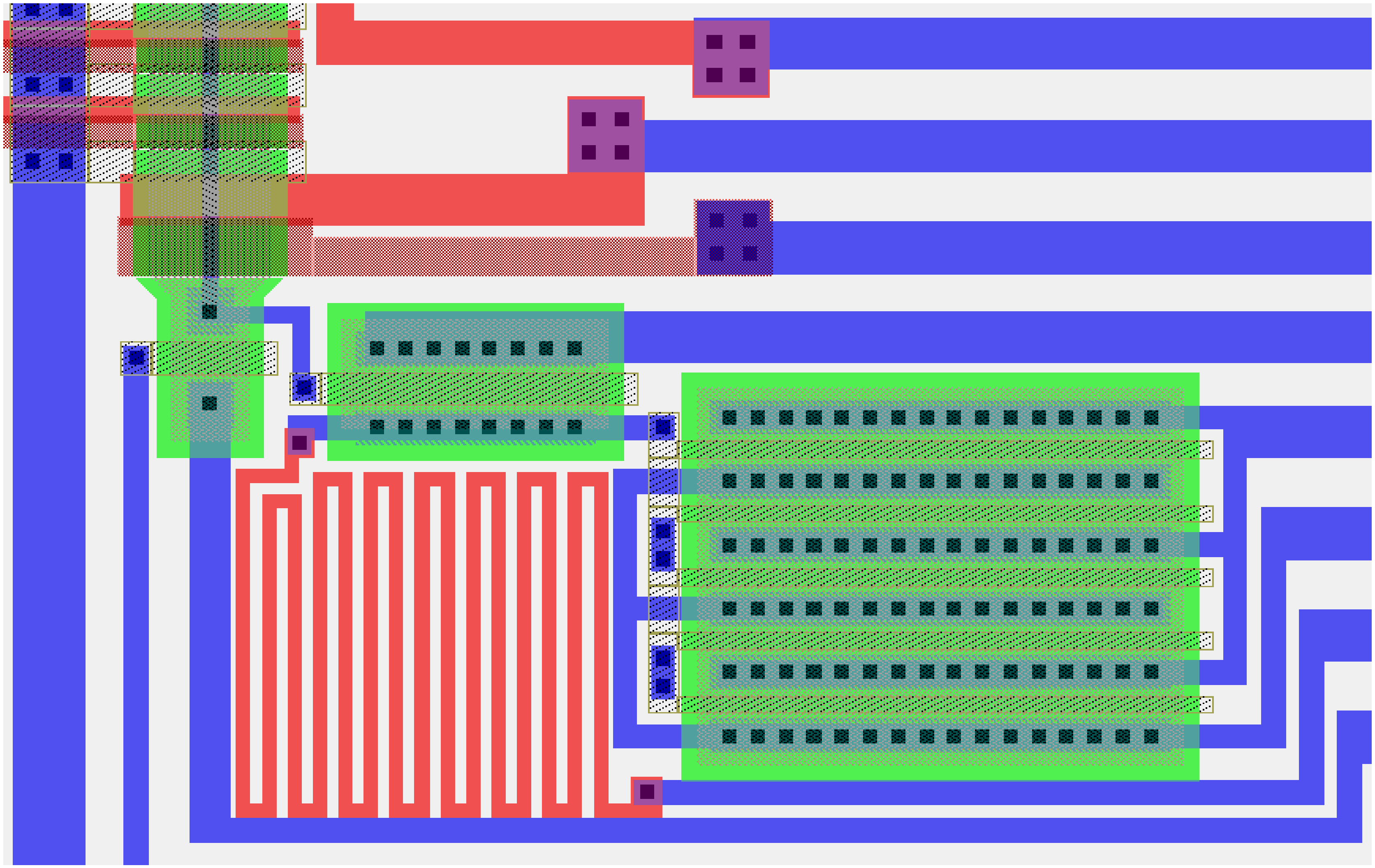
Channel resistor temperature dependence



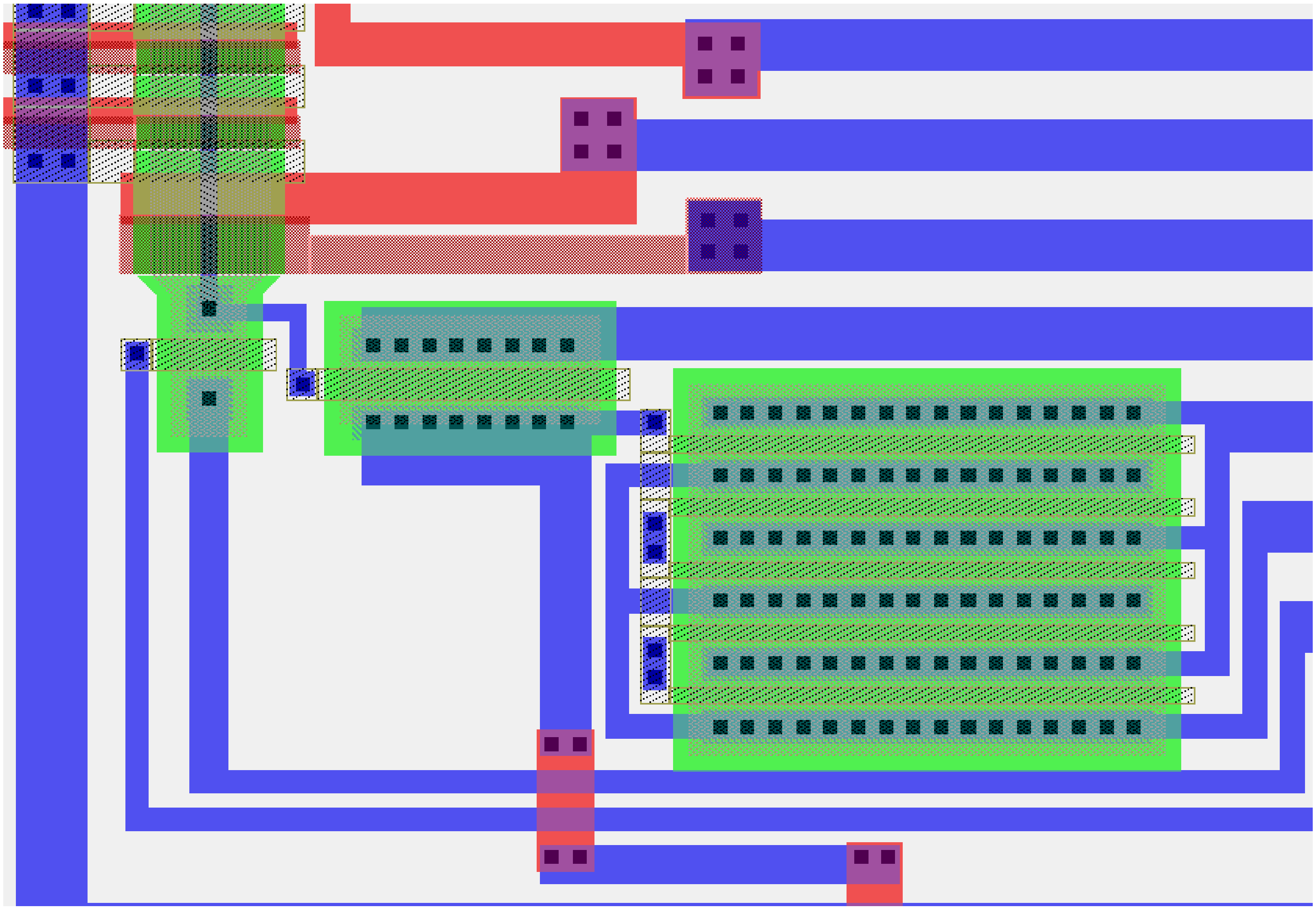
Transistor load



Gate poly load resistor



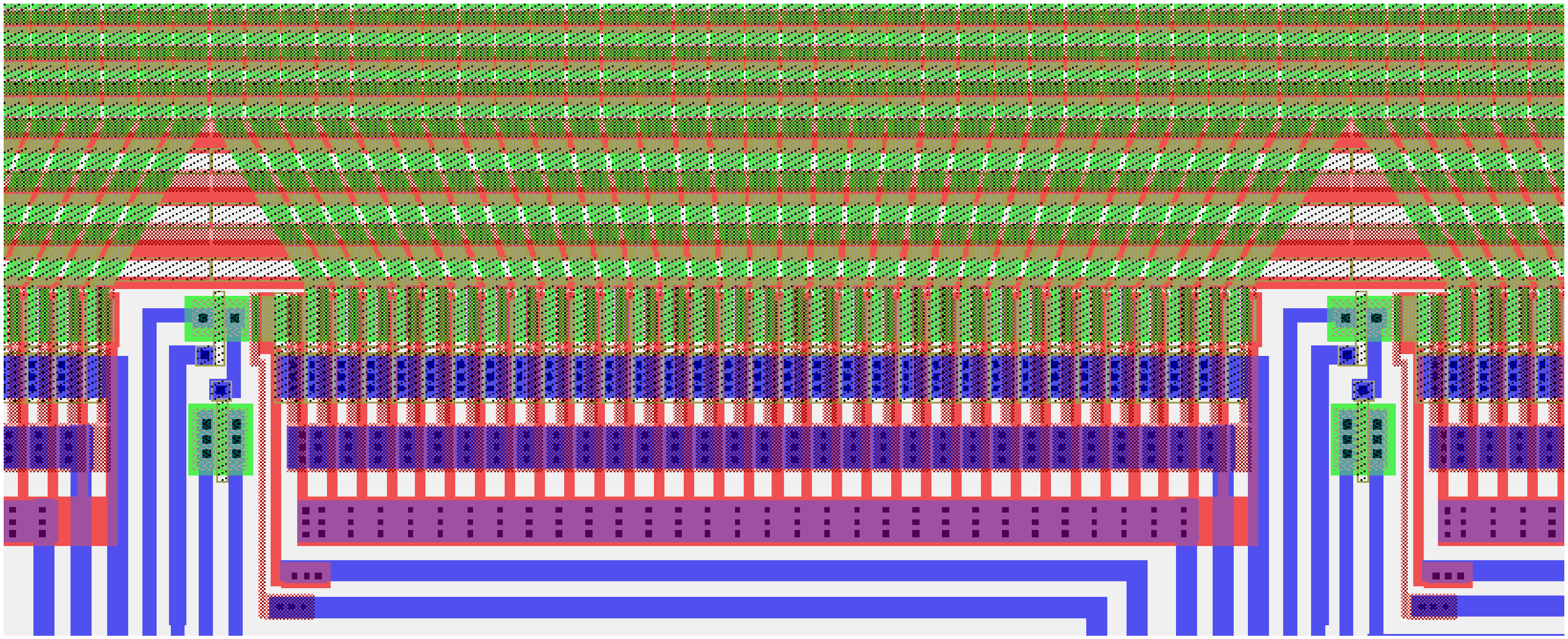
External resistor load



Key R&D Issues / Work in Progress

- Commercialization
  - — Experience with 300 μm thick, 150 mm diameter wafers
  - — Resistivity attainable with 150 mm wafers
    - LBNL 100 mm wafers > 10 kΩ-cm
    - Foundry 150 mm wafers 4.4 – 7.6 kΩ-cm
    - Depletion voltage α $(\text{Resistivity})^{-1}$
- Ground-based astronomy efforts
  - — 2048 x 2048 for Hamilton Spectrograph at Lick Observatory (engineering runs)
  - — 800 x 1980 for KPNO RC Spectrograph (2001B semester in shared-risk mode)
  - — 2048 x 4096 development with Lick CCD Testing Lab for Keck ESI Spectrograph
- Proton irradiations at LBNL 88” Cyclotron
- Collaboration with JPL on δ-doping for back illumination
  - — Low temperature process (MBE) done on finished device
  - — Does not require foundry processing of thinner than normal wafers
  - — Arbitrarily thin for good point spread function

9 mm pixel issues



Multi-amplifier CCD designed at JPL. The serial register is wide for high-speed readout while the pixel size is smaller than in the main array to allow area for the amplifiers.